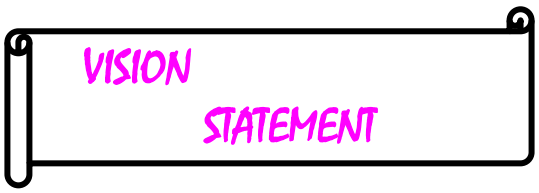
II-B.Tech–II SEM

STUDENT HANDBOOK

A.Y.2016-17

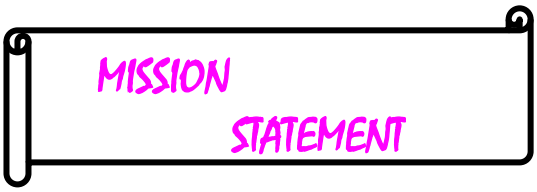
Dept. of ECE

MARRI LAXMAN REDDY
INSTITUTE OF TECHNOLOGY & MANAGEMENT
(Approved by AICTE-New Delhi, Accredited by NAAC with 'A' & Affliated to JNTU, Hyderabad)
Recognised Under Section 2(f) & 12(B) of The UGC act, 1956



VISION STATEMENT OF MLRITMM

To establish as an ideal academic institution by graduating talented engineers to be ethically strong, competent with quality research and technologies.



MISSION STATEMENT OF MLRITMM

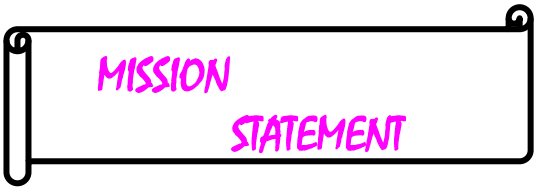
- Utilize rigorous educational experiences to produce talented engineers.
- Create an atmosphere that facilitates the success of the students.
- Prudent and accountable resource management.
- Program that integrate global awareness, communication skills and Leadership abilities.
- Education and Research partnership with institutions and industries for preparing students for interdisciplinary research.
- Successful alumni in their profession at global level

QUALITY POLICY OF MLRITMM

Aspire to establish a system, which would improve the quality of education, teaching-learning and training process on continuous basis and ultimately develop the institute as a center of excellence.

VISION STATEMENT OF DEPARTMENT

Imparting quality technical education through research, innovation and team work for a lasting technology development in the area of Electronics and Communication Engineering.



MISSION STATEMENT OF DEPARTMENT

- To develop a strong centre of excellence for education and research with excellent infrastructure and well qualified faculties to instill in them a passion for knowledge.
- Establish a unique learning environment to face the various challenges in their profession.
- Promote establishment of centers of excellence, nurture the spirit of innovation.
- Provide ethical and value based education.
- Enable students to develop skills to solve complex technological problems, multidisciplinary activities.

Our Pioneers...

MARRI LAXMAN REDDY – CHAIRMAN

Sri Marri Laxman Reddy, the Founder Chairman of MLR Institutions – Marri Laxman Reddy Institute of Technology and Management, MLR Institute of Pharmacy and Marri Laxman Reddy Institute of Technology and Management. He is also Founder Chairman of St. Martin's Engineering College and St. Martins Schools at Balanagar, Chintal (HMT) and Malkajgiri who has been in the field of education from last 22 years with the aim spreading quality education among children at the school and college level. He is a veteran Athlete International repute.

MARRI RAJASEKHAR REDDY – SECRETARY

Mr. M. Rajasekhar Reddy, a person with remarkable abilities and great acumen and a dynamic leader. He is known to be the dynamic mentor of Marri Laxman Reddy Institute of Technology and Management & Management who is always on the sprit to take the institute to newer levels in every aspect of an "Ideal Institution" and strives hard to make every dream a reality. He like his father Mr. M. Laxman Reddy, has a credit of establishing Institute of Aeronautical Engineering adding a new flavor to St. Martins group of Institutions, Vidyanjali Grammer School. His ability to turn adversities into opportunities is unquestionable.

The Secretary has a vision of establishing Marri Laxman Reddy Institute of Technology and Management & Management as a brand. He is striving hard to initiate various industry oriented programs for the benefit of the students and he envisions his student to be present at the top most position in the industry.

Dr. K. VENKATESWARA REDDY – PRINCIPAL

Dr.K.Venkateswara Reddy, M.Tech., Ph.D., MISTE, the Principal, Marri Laxman Reddy Institute of Technology& Managemnt, is a young and dynamic Professor of CSE, has 15 years of Teaching, Research and Administrative experience in reputed engineering colleges & industry. In 15 years of experience served various positions from Asst. Professor to Principal. He received "The Great Mind Challenge - 2013, TGMC Mentor Award".

Dr.K.V.Reddy contributed immensely for the growth of institutes by introducing the disciplinary innovative in the life style of under graduate engineering students. He has established Institute-Industry Interaction and Research & Development cells in the institute.

Research & Guidance: Dr.K.V.Reddy has Published 22 research papers at national and international level in the areas of mathematical modeling and computing simulations such as advanced numerical solutions for Thermoelasticity and in farming the innovative researh explorations in cloud computing, network security, MANET and other emerging fields of computer science

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ECE STUDENT HANDBOOK

II B Tech –II Semester

Academic Year: 2016-2017

Document No: MLRITMM/ECE/SHB/2016 **Date of Issue: Jun'2016**

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➢ 1. COURSE CALENDAR OF THE YEAR

Registrations	04-07-2016	
1st spell of Instructions	04-07-2016	16-07-2016 (2 Weeks)
I B.Tech II Sem. Supplementary Examinations	18-07-2016	14-07-2016 (1 week 3days)
1st spell of Continuation	28-07-2016	07-09-2016 (6 week)
I mid term exams	08-09-2016	14-09-2016 (1 week)
2nd spell of Instructions	15-09-2016	04-10-2016(2 weeks 5days)
Dussehara Holidays	05-10-2016	12-10-2016 (1 week)
2nd spell Continuation	13-10-2016	17-11-2016(5 weeks 1day)
II mid term exams	18-11-2016	24-11-2016 (1 week)
Preparations & Practical examinations	25-11-2016	30-11-2016 (1 week)
End examinations	01-12-2016	14-12-2016 (2 weeks)
Semster Break	15-12-2016	28-12-2016 (2 weeks)
II B.Tech I Sem. Adv.Supplementary Examinations	29-12-2016	07-01-2017 (1 week 3 days)
II. B.Tech II Sem Class work commencement.	09-01-2017	

2.II YEAR II SEMESTER COURSE STRUCTURE

CODE	SUBJECT	T	P	C
54019	Principles of Electectrical Engineering	3+1*	-	3
54020	Electronic Circuit Analysis	4+1*	-	4
54021	Pulse and Digital Circuits	4+1*	-	4
54010	Switching Theory and Logic Design	4+1*	-	4
54011	EM Theory and Transmission Lines	4+1*	-	4
54606	Electrical Engineering Lab`	-	3	2
54607	Electronic Circuit Analysis Lab	-	3	2
54608	Pulse & digital Circuits Lab	-	3	2
	Total	**19+5***	**9**	**25**

Note: All End Examinations (Theory and Practical) are of three hours duration.

T – Theory P- Practical C – Credits

3. PRINCIPLES OF ELECTRICAL ENGINEERING

3.1 JNTUH SYLLABUS

UNIT I TRANSIENT ANALYSIS (First and Second Order Circuits): Transient response of RL, RC and RLC Series circuits for DC excitations, Initial connections, Solution using Differential Equations approach and Laplace Transform Method.

UNIT II TWO PORT NETWORKS : Impendence Parameters, Admittance Parameters Hybrid Parameters, Transformation(ABCD) Parameters, Conversion of one Parameter to another, Condition for Reciprocity and Symmetry, Interconnection of Two Port networks in Series, Parallel and Cascaded configurations, Image Parameters, Illustrative problems.

UNIT III FILTERS : Classification of Filters, Filter Networks, Classification of Pass band and Stop band, Characteristic Impedance in Pass and Stop Bands, Constant k Low Pass Filter, High Pass Filter, m-derived T-section, Band Pass Filter and Band Elimination filter, Illustrative Problems.

UNIT IV SYMMETRICAL ATTENUATORS : Symmetrical Attenuators – T type Attenuator, δ type Attenuator, Bridged T type attenuator, Lattice Attenuator.

UNIT V DC GENERATORS : Principle of Operation of DC Machine, EMF equation,Types of Generators, Magnetization and Load Characteristics of DC Generators.

UNIT VI DC MOTORS : Types of DC Motors, Characteristics of DC Motors, Losses and Efficiency, Swinburne's Test, Speed Control of DC Shunt Motor, Flux and Armature Voltage control methods.

UNIT VII TRANSFORMERS AND THEIR PERFORMANCE : Principle of operation of single phase Transformer, Types, Constructional Features, Phasor Diagram on No Load and Load, Equivalent Circuit, Losses and Efficiency of Transformer and Regulation, OC and SC Tests, Predetermination of Efficiency and Regulation(Simple problems).

UNIT VIII SINGLE PHASE INDUCTION MOTORS : Principle of Operation of Shaded Pole motors, Capacitor motors, AC Servomotor, AC Tachometers, Synchros, Stepper Motors, Characteristics.

Text Books :

1. Fundamentals of Electric Circuits - Charles K.Alexander, Mathew N, O. Sadiku, 3 ed., 2008, TMH.
2. Network Analysis – A Sudhakar, Shyammohan S. Palli, 3 ed., 2009, TMH.
3. Introduction to electrical engineering – M.S.Naidu and S.Kamakshaiah., 2008, TMH..

3.2 UNIT WISE PLANNER FOR ACADEMIC YEAR 2013 - 2014

Subject: Principles of Electrical Engineering

Unit No.	Date Planned	Date Conducted	Remarks
I			
II			
III			
IV			
V			
VI			
VII			
VIII			

3.3 SESSION PLANNER

UNIT	LECTURE NO.	TOPIC	Date Planned	Date Conducted	Text / Ref. Book
I	L1	Introduction			T1
	L2	Transient response of RL Series circuits for DC excitations, Initial conditions(Solution using Differential Equations approach)			T1
	L3	Transient response of RC Series circuits for DC excitations, Initial conditions, (Solution using Differential Equations approach)			T1
	L4	Transient response of RLC Series circuits for DC excitations, Initial connections,(Solution using Differential Equations approach)			T1
	L5	Problems			T1&T2
	L6	problems			
	L7	Introduction of Laplace Transform Method.			T1&T2
	L8	Transient response of RL Series circuits for DC excitations. Transient response of RC Series circuits for DC excitations.(Laplace Transform Method)			T1

	L9	Transient response of RLC Series circuits for DC excitations.(Laplace Transform Method)			T1
	L10	Class test			T1
II	L11	Introduction			T1
	L12	Impedance Parameters			T1
	L13	Admittance Parameters			T1
	L14	Problems			T1
	L15	Hybrid Parameters, problems			T1
	L16	Transmission(ABCD) parameters, Problem			T1
	L17	Conversion of one parameter to another, Conditions for			T1
	L18	Interconnection of two ports in series, parallel and cascaded			T1
	L19	Image parameters			T1
	L20	Class test			
III	L21	Classification of Filters, Filter Networks, Equations of Filter			T1
	L22	Equations of Filter Networks			T1
	L23	Classification of Pass band and Stop band, Characteristic			T1
	L24	Constant k Low Pass Filter Problem			T1
	L25	Constant k High Pass Filter, Problem			T1
	L26	m- Derived T section filter, Low pass, problem			T1
	L27	High pass filter, problem			T1

	L28	Band Pass Filter, Band Elimination Filter .			T1
	L29	Class test			
IV	L30	Attenuators, T-Type Attenuators			T1
	L31	Pi- Attenuator, problem			T1
	L32	Bridged T-Type Attenuator, problem.			T1
	L33	Lattice Attenuator, problem			T1
	L34	Class test			
V	L35	Principle of operation of DC Machine, Construction			T3
	L36	Constructional details of DC Machine.			T3
	L37	E.M.F Equation			
	L38	Types of Generators			T3
	L39	Magnetization and Load Characteristics of DC			T3
	L40	Problems			T3
	L41	Class test			
VI	L42	Operation of DC Motor			T3
	L43	Types of DC Motors			T3
	L44	Characteristics of DC Motors			T3
	L45	Losses and Efficiency.			T3
	L46	Swinburne's Test,			T3
	L47	Speed control of DC Shunt Motor.			T3
	L48	Armature and Flux Voltage Control method			
	L49	Class test			T3
VII	L50	Principle of operation of single phase Transformer			T3
	L51	Types, Constructional Features			T3

	L52	Phasor Diagram on No Load.			T3
	L53	Phasor Diagram on Load .			
	L54	Equivalent Circuit			T3
	L55	Losses and Efficiency of Transformer and Regulation			T3
	L56	OC and SC Tests			T3
	L57	Predetermination of Efficiency and Regulation			T3
	L58	Class test			T3
VIII	L59	Principle of Operation of Shaded Pole motors			T3
	L60	Capacitor motors			T3
	L61	AC Servomotor, AC Tachometers			T3
	L62	Synchros			T3
	L63	Stepper Motor's Characteristics			T3
	L64	Class test			

3.4. QUESTION BANK

3.4.1 UNIT -I

3.4.1.1 DESCRIPTIVE QUESTIONS

1. What is the significance of time constant of R-C circuit?

2. Find the DC response of a series R-C circuit ?

3.Determine the current i(t) in series RLC circuit consisting of R=5Ω,L=0.5H and C=0.25f. When the applied v(t) is a ramp voltage 12r(t-2).Assume that the circuit is initially relaxed (Use Laplace Transform Method)

4. Obtain S-Domain equivalent for the following elements

- Resistance (R)
- Inductance with initial current Io
- Capacitor with initial voltage Vo give the relevant equations

5. In a series RL circuit with R=3Ω and L=1H a DC Voltage Vi=50V is applied at t=0 find the transient response of current?

ASSIGNMENT QUESTIONS:

1 Explain why voltage across capacitor cannot change instantaneously?

2. What are the different ways defining time constant ?

3.Obtain the current (RLC series circuit) for t>0, using time domain approach.

3.4.1.2OBJECTIVE QUESTIONS

1.The time constant of RL circuit is.....

2.Inductor does not allow sudden changes in .....

3.Transient current in an RLC circuit is oscillatory when.....

4.The time constant of RC circuit is.....

5.When a series RL circuit is connected to a voltage V at t=0, the current passing through the inductor L at t=0+ is .....

6.Capacitor does not allow sudden changes in.....

7.The laplace transform of a unit step function is.....

8.The laplace transform of a impulse function is.....

3. The final value theorem is used to find the.....

10.When a series RC circuit is connected to a voltage V at t=0, the current passing through the circuit at t=0+ is .....

3.4.1.3 TUTORIAL TOPICS

1.Find the DC response of series R-Ccircuit

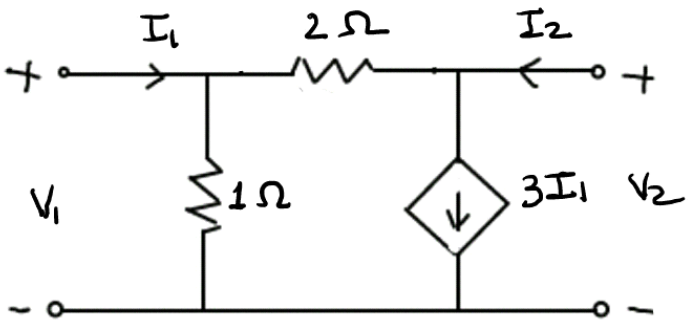
2.Find the DC response of series R-L-C circuit (Laplace transform approach)

3.4.2 UNIT-II

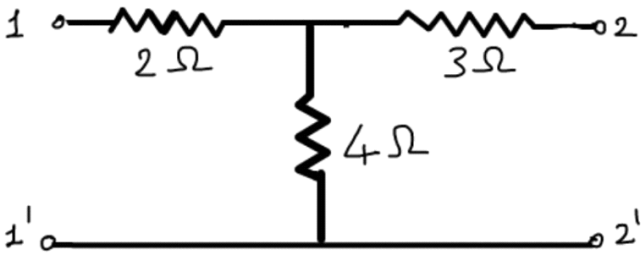
3.4.2.1 DESCRIPTIVE QUESTIONS

1.What parameters are used to deal with two ports connected in cascade and explain about two 2- port network cascade combination ?

2. Find Z-parameters for the circuit shown in figure .



3. What is meant by port? Explain about two port network.
4. Determine Image parameters of the T-network shown in figure

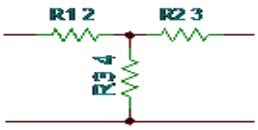


5. Explain about the Image parameters with correlation to 2-port networks
6. Derive the Image impedances for symmetrical and reciprocal networks

ASSIGNMENT QUESTIONS:

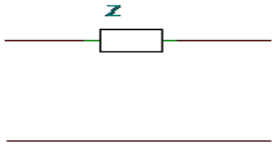
1. Derive equations for Z-parameters in terms of Y-parameters.

2.Find all(Z, Y, ABCD, h) parameter values of the below circuit



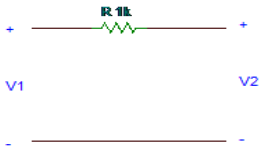
3.4.2.2 OBJECTIVE QUESTIONS

1. Which of the following parameters do not exist for the two port network shown in fig.



a) ABCD b) Y c) h d) Z

1 .Find the Z parameters of the following



3.Find the Y- Parameters for theFIg-2

a) b) c) do not possible d) none.

4. Find the Z parameters of Fig 3.

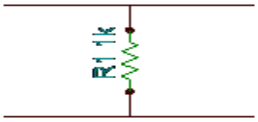


Fig 3

a) b) c) d) none.

5. Find the Y parameters of Fig 3.

a) b) c) d) do not possible

6 . For a two port network z11y11 =

a) Z12Y21 b) Z21Y12 c) Z22Y11 d) none

7. Two two port networks are cascaded. The combination is to be represented as a single two-port network. The parameters of the network are.

a) Z-parameter matrix b) Y-parameter matrix c) h-parameter matrix d)ABCD-parameter matrix

8. For a two port network to be reciprocal

a) Z11=Z22 b) Y12 = Y21 c) h22 = h12 + h21 d) AD - BC=0

8. Two two port networks are parallel connected. The combination is to be represented as a single two-port network. The parameters of the network are.

a) Z-parameter matrix b) Y-parameter matrix c) h-parameter matrix d)ABCD-parameter matrix

9. A two port device is defined by the following pair of equations

I1 = 2V1 + V2 and I2 = V1 + V2 the impedance parameters (Z11,Z12,Z21,Z22) are given by

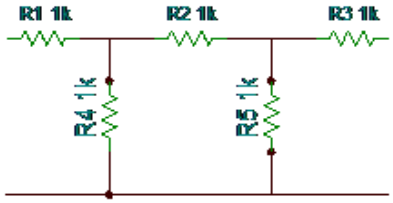
a) (2,1,1,1) b) (1,-1,-1,2) c) (1,1,1,2) d) (2,-1,-1,1)

10. The short circuit admittance matrix of a two-port network is , The two port network is

a) Non-reciprocal and passive b) Non-reciprocal and active

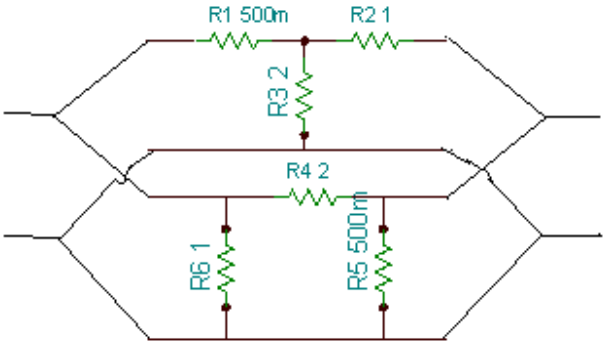
c) Reciprocal and passive d) Reciprocal and active

11. Find the value of h12 of given figure below.



a) 0.125 b) 0.167 c) 0.625 d) 0.25

12. Find the Y-Parameters of equivalent network.



a) b) c) d)

13. Which parameters are suitable to minimize Cascaded Networks.

a) Z b) Y c) h d) ABCD

14. Which parameters are suitable to minimize Series Networks

a) Z b) Y c) h d) ABCD

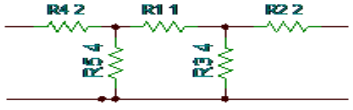
15) Which parameters are suitable to minimize Parallel Networks

a) Z b) Y c) h d) ABCD

4.4.2.1 TUTORIAL QUESTIONS

• 1. Write every parameter in terms of all other parameters.

• 2.Find all(Z, Y, ABCD, h) parameter values of the below circuit



3.4.3 UNIT-III

3.4.3.1 DESCRIPTIVE QUESTIONS

1. What is Filter and Explain various types of filters

2.Design a high pass filter with a cut off frequency of 2kHz with a terminated design impedance of 800 ohm.

3.Derive the propagation constant (γ) of symmetrical T- network

4. Design a m-derived low pass filter having a cut off frequency of 1kHz,design impedanceof 400 ohm, and the resonant frequency is 110Hz .

5..Derive the characteristic impendence of a symmetrical π-network and express in terms of open circuit impedance and short circuit impendence.

6. A π- section filter having c/2=14uf, c/2=14uf and L=15mH calculate the cut off frequency and the value of nominal impedance in the pass band.

ASSIGNMENT QUESTIONS

1. Design a Constant – k Low pass filter with cut-off frequency 100KHz,having a Design Impedance 400Ω, Draw the T type and π type Networks with values.
2.Design a Constant – k High pass filter with cut-off frequency 1KHz,having a Design Impedance 500Ω, Draw the T type and π type Networks with values.

3.4.3.2 OBJECTIVE QUESTIONS

1. The basic type of filter is _ _ _ _ _

a)m-Derived Filter b) Constant-k Filter c) a and b d) none

2) Z1Z2= _ _ _ _ _

a)K2 b) K c) m d) none

3.Filter elements are only

a)Capacitors and Resisters b) Resisters and Inductors c) Capacitors and Inductors d) none

4. Attenuation constant and phase shift constants in Stop band are

a) increases gradually and zero b) both increases gradually c) both zero d) zero and increases gradually

5. 10 Decebels =_ _ _ _ _

a) 10 log10x b) 100 log10x c) 10 log 2 x d) none

6. Attenuation constant and phase shift constants in Pass band are

a) increases gradually and zero b) both increases gradually c) both zero d) zero and increases gradually

7. Band Pass filter is _ _ _ _ _.

a) High Pass Filter followed by Low Pass Filter b) Low Pass Filter followed by High Pass Filter

c) not possible d)none.

8. Series L and C Circuit provides _ _ _ _ _ impedance at resonance.

a) ∞ b) -∞ c) 0 d)none

9. Series R,L and C Circuit provides _ _ _ _ _ impedance at resonance.

a) ∞ b) -∞ c) 0 d)R

10.Parallel L and C Circuit provides _ _ _ _ _ impedance at resonance.

a) ∞ b) -∞ c) 0 d)none

11. Series R,L and C Circuit provides _ _ _ _ _ impedance at resonance.

a) ∞ b) -∞ c) 0 d)R

3.4.3.3 TUTORIAL TOPICS

1. Design a m-Derived Low pass filter with cut-off frequency 100KHz,having a Design Impedance 400Ω, Draw the T type and π type Networks with values.
2. Design a m-Derived High pass filter with cut-off frequency 10KHz,having a Design Impedance 500Ω, Draw the T type and π type Networks with values

3.4.4 UNIT-IV

3.4.4.1 DESCRIPTIVE QUESTIONS

1. Design a symmetrical T-type Attenuator

2. An attenuator composed of symmetrical π- Section having series arm each of 100 ohm, and shunt arm of 300 ohm , Calculate the characteristic impedance and attenuation per Section

3.Design a symmetrical π -type Attenuator

4. Design a symmetrical Lattice attenuator to operate into a resistance of 500 ohm, and to provide attenuation of 15 db

5.Design a symmetrical Lattice -type Attenuator

6. Design a symmetrical T -type attenuator to operate into a resistance of 400 ohm, and to provide attenuation of 20 db .

ASSIGNMENT QUESTIONS

1.Derive the element equations of π-Type Attenuator.

2.Derive the equation for R2 in Lattice Attenuator

3.4.4.2 OBJECTIVE QUESTIONS

1. Application of attenuator is _____.

a)To provide Phase Shift b) To provide Attenuation c) To provide both a and b d) none

2. R1 in T type attenuator is _____.

a)Ro(N - 1) / (N + 1)b) Ro(N + 1) / (N - 1) c) Ro(N - 1) / (N2 - 1) d) Ro 2N / (N2 - 1)

3.R2 in π Attenuator is _____.

a) Ro(N - 1) / (N + 1) b) Ro(N + 1) / (N - 1) c) Ro(N - 1) / (N2 - 1) d) Ro 2N / (N2 - 1)

4.R1 in π Attenuator is _____.

a) Ro(N - 1) / (N + 1) b) Ro(N + 1) / (N - 1) c) Ro(N - 1) / (N2 - 1) d) Ro (N2 - 1)/2N

5.R2 in T Attenuator is _____.

a) Ro(N - 1) / (N + 1) b) Ro(N + 1) / (N - 1) c) Ro(N - 1) / (N2 - 1) d) Ro 2N / (N2 - 1)

6. R2 in lattice Attenuator is _____.

a) Ro(N - 1) / (N + 1) b) Ro(N + 1) / (N - 1) c) Ro(N - 1) / (N2 - 1) d) Ro 2N / (N2 - 1)

7. R2 in lattice Attenuator is _____.

8. Ro(N - 1) / (N + 1) b) Ro(N + 1) / (N - 1) c) Ro(N - 1) / (N2 - 1) d) Ro 2N / (N2 - 1)

9. RA in Bridged T Attenuator is _____

10. Ro(N - 1) b) Ro / (N - 1) c) Ro(N - 1) / (N2 - 1) d) Ro 2N / (N2 - 1)

11.RB in Bridged T Attenuator is _____.

12. Ro(N - 1) b) Ro / (N - 1) c) Ro(N - 1) / (N2 - 1) d) Ro 2N / (N2 - 1)

13.Design a symmetrical bridged-T attenuator with an attenuation of 20dB into a load of 500Ω. RA, RB, are

14.a)4.5k b) 55 Ω c) 4.5k,55 Ω d) none.

Design a Lattice attenuator with an attenuation of 20dB into a load of 800Ω. R1 R2 are

a) 654.54 Ω b) 977.77 Ω c) both a and b d) none.

15.Design π-type attenuator with 20 dB attenuation, and to have a characteristic impedance of 100Ω

a)495 Ω b) 122.22 Ω c) both a and b d) none

16. Design T-type attenuator with 60 dB attenuation, and to have a characteristic impedance of 500Ω

a) 499 Ω b) 1 Ω c) both a and b d) none

3.4.4.3 TUTORIAL TOPICS

1. Design a symmetrical Bridged T -type Attenuator.

2.Design a symmetrical π -type attenuator to operate into a resistance of 600 ohm, and to provide attenuation of 60 dB
3.Design a symmetrical bridged-T attenuator with an attenuation of 40 dB and terminated into a load of 400 Ω.

3.4.5 UNIT-V

3.4.5.1 DESCRIPTIVE QUESTIONS

1. explain the working principle of operation of a d.c.generator.

2. explain the types of a d.c generator.

3. derive the e.m.f equation of a d.c.generator.

4.draw the block diagram of a d.c generator and explain its parts

ASSIGNMENT QUESTIONS

1.draw the block diagram of a d.c generator and explain its parts.

2.What are separately and self exited D.C generators? Explain them with help of neat sketches.

3.4.5.2 OBJECTIVE QUESTIONS

1. . Mechanical Energy Converted to Electrical energy which of the following

(A)Generator (B) Motor (C) Both A&B (D) None

2.The direction of induced e.m.f and hence current in a conductor can be determined by

(A)Lenz's Law (B) Fleming's Right hand rule (C) Both A&B (D) Fleming's Left hand rule

3.In DC Machine which Induced e.m.f is suitable

(A)Statically induced e.m.f (B) dynamically induced e.m.f (C) there is no e.m.f (D) None

4. The function of the commutator

(A)Ac to dc (B) dc to ac (C) both A&B (D) None

5. Brushs are made up of

(A)Carbon (B) Silicon (C) copper (D) Mild steel

6. Armature Reaction is related to

(A)Main flux &Armature flux (B) only Main flux (C) only Armature flux None

7. Which is suitable for Electric Traction?

(A)Series Motor (B) Shunt Motor (C) Compound Motor (D) Dc Generator

8. Which of the following are Iron Losses?

(A)Copper losses (B) Mechanical losses (C) friction loss (D) Eddy current losses

9. The Basic Principle in dc generator is

(A)Electro Magnetic Induction (B) Flemings Left hand rule (C) Law of conservation Energy

10. DC generators are classified based on_____

3.4.5.3 TUTORIAL TOPICS

1.Pole generator has 32 conductors. Average emf induced in each conductor is 1.5 V and carries a current of 4 A. Calculate the power generated in the machine (a) If the machine is wave wounded, and (b) If the machine is lap connected.

2. A long shunt compound generator supplies a load current of 75 A at 440 V, the resistance of armature, series field and shunt field are 0.02Ω, 0.01 Ω and 150 Ω respectively. Calculate the generated emf; assume 1V per brush for contact drop

3.4.6 UNIT-VI

3.4.6.1 DESCRIPTIVE QUESTIONS

1.Explain the working principle of operation of a motor.

2.Explain the various types of motors.

3.Derive the expression for torque of a d.c motor.

4.Explain how to calculate efficiency and losses in a d.c motor

ASSIGNMENT QUESTIONS

1. Derive the Torque Equation of DC Motor.
2. Explain about different types of DC Motors?

3.4.6.2 OBJECTIVE QUESTIONS

1). . Swinburne's test conduct on DC Shunt Machine is

(A) No load (B) Full load (C) Both A&B (D) None

2. Armature windings are made up on

(A)Copper (B) Mild wire (C) Aluminum (D) None

3. Which of the following is unit of Torque is

(A)Newton-meter (B) watts (C) Length (D) None

4.the starting resistance of a D.C. motor is generally

(A)Low (B) around 500 ohm (C) 100 ohm (D) infinitely large

5. Small DC motors up to 5 H.P. Usually

(A) 2 poles (B) 4poles (C) 6poles (D) 8poles

6.Swinburne's test conduct on DC Shunt Machine is

(A) No load (B) Full load (C) Both A&B (D) None

7. Armature windings are made up on

(A)Copper (B) Mild wire (C) Aluminum (D) None

8. Which of the following is unit of Torque is

(A)Newton-meter (B) watts (C) Length (D) None

9.the starting resistance of a D.C. motor is generally

(A)Low (B) around 500 ohm (C) 100 ohm (D) infinitely large

10. Small DC motors up to 5 H.P. Usually

(A) 2 poles (B) 4poles (C) 6poles (D) 8poles

3.4.6.3 TUTORIAL TOPICS

1.Explain the Characteristics of DC Motors

2. Explain the working principle of DC Motor.

3.4.7 UNIT-VII

3.4.7.1 DESCRIPTIVE QUESTIONS

1.explain the working principle of a one phase transformer.

2.explain the equivalent circuit of a one phase transformer.

3.explain oc and sc test on a single phase transformer.

4.what are the losses and how to minimize the losses in a transformer

ASSIGNMENT QUESTIONS

1. Derive the EMF equation of Single phase Transformer.
2.Explain about Transformer equivalent circuit

3.4.7.2 OBJECTIVE QUESTIONS

1). Induced e.m.f in a coil is directly proportional to

(a) Rate of change of flux linkage

(b) Rate of change of charge

(c) Depends on the material used

(d) Rate of change of current

2). The transformer rating is

(a) KW (b) KVA (c) KV (d) WATT

3). The transformer transforms

(a) Frequency (b) Voltage (c) Current (d) Voltage & Current

4). The main purpose of using Core in transformer is to

(a) Decrease Iron losses (b) Prevent Eddy current losses

(c) Eliminate Magnetic hysteresis

(d) Decrease Reluctance of the Common magnetic circuit

5). The transformer cores are laminated in order to

(a) Simplify its constructions (b) Minimize Eddy current losses

(c) Reduce cost (d) Reduce Hysteresis losses

6). The Primary and Secondary induced E.M.Fs E1 & E2 in a Two winding transformer are always

(a) Equal in magnitude (b) Anti-Phase with each other

(c) In-Phase with each other (d) Determined by load on transformer Secondary

7). The Step-up transformer increases

(a) Voltage (b) Current (c) Power (d) Frequency

8). The Step-down transformer decreases

(a) Voltage (b) Current (c) Power (d) Frequency

9). The main purpose of performing open circuit test on a transformer is to measure Its

(a) Copper losses (b) Iron losses (c) Total losses (d) Insulation resistance

10). The main purpose of performing short circuit test on a transformer is to measure Its

(a) Copper losses (b) Iron losses (c) Total losses (d) Insulation resistance

11). In a transformer the load is connected to

(a) Primary (b) Secondary (c) Both (a) & (b) (d) None

12). The efficiency of the transformer depends on

(a) Input power (b) Losses in transformer (c) Power factor (d) All the above

3.4.7.3 TUTORIAL TOPICS

1. Explain about Iron and Copper Losses in Transformer.
2. Explain the working principle of DC Motor

3.4.8 UNIT-VIII

3.4.8.1 DESCRIPTIVE QUESTIONS

1.Explain the constructional features and principle of operation of a single phase induction motor.

2.Explain the constructional details of shaded pole single phase induction motor.

3.Explain about various types of capacitor motors.

4.Why single phase induction motors are not self starting?

5.Explain the cross field theory of asingle phase induction motor?

ASSIGNMENT QUESTIONS

1. Derive the Torque Equation of DC Motor.

2. Explain about Capacitor Split-Phase Starting of Single phase induction motor.

3.4.8.2 OBJECTIVE QUESTIONS

1.The starting of the motor requires generation of .....

2.Large number of poles in tachogenerators results in.....

3.The single phase motor starting torque is zero because of.....

4.When compared to full-step drive ,haif-step drive requires.....

5.When compared to full-step drive ,haif-step drive produces.....

6.The starting winding in a single phase motor is placed in.....

7.The torque exerted by the rotor magnetic field of a PM stepper motor is called.....

8.The basic requirement of a servo motor is that it must produce high torque at .....

9.In control applications,synchro pair is used for.....

10.For a two value capacitor motor ,the type of capacitor used for the running purpose is.....

3.4.8.3 TUTORIAL TOPICS

1.Explain how a capacitor start split phase induction motor develops a rotating magnetic field.

2.Explain the working principle of Single phase Induction motor

4. ELECTRONIC CIRCUIT ANALYSIS

4.1. JNTUH SYLLABUS

Unit- I: Single Stage Amplifiers Classification of amplifiers, Distortion in amplifiers Analysis of CE,CC,CB Configurations with simplified Hybrid model, Analysis of CE amplifiers with emitter resistance and Emitter follower, Millers Theorem and its dual, Design of single stage RC Coupled Amplifier using BJT

Unit- II: Multi Stage Amplifiers Analysis of Cascaded RC Coupled BJT Amplifiers, Cascode Amplifiers, Darlington pair, Different Coupling Schemes used in Amplifiers-RC Coupled Amplifier, Transformer Coupled Amplifier, Direct Coupled Amplifier

Unit- III: BJT Amplifier – Frequency Response Lagarithms, Decibles, General Frequency Considerations, Frequency response of BJT Amplifier, Analysis at Low and High Frequencies, Effect of coupling and bypass Capacitors, The Hybrid – pi (?) – Common Emitter Transistor Model, CE Short Circuit Current Gain, Current Gain with Resistive load, Single Stage CE Transistor Amplifier Response, Gain-Bandwidth Product, Emitter Follower at higher frequencies.

Unit- IV: MOS Amplifier Basic concepts, MOS Small signal model, common source amplifier with Resistive load, Diode connected Load and Current Source Load, Source follower, Common Gate stage Cascode and Folded Cascode Amplifier and their Frequency response.

Unit- V: Feedback Amplifier Concept of Feedback, Classification of Feedback Amplifiers, General characteristics of a Negative Feedback amplifiers, Effect of feedback on Amplifier Characteristics, Voltage Series, Voltage Shunt, Current Series and Current Shunt Feedback Configurations, Illustrative Problems.

Unit- VI: Oscillators Classification of oscillators, Conditions for Oscillations, RC Phase Shift Oscillator, Generalized analysis of LC Oscillators – Hartley, and colpitts Oscillators, Wien-Bridge & Crystal Oscillators, Stability of Oscillators.

Unit- VII: Large Signal Ampli fiers Classification, Class A Large signal Ampli fiers, Transformer Coupled Class A Audio Power Amplifier, Efficiency of Class A Amplifier, Class B Amplifier, Efficiency of Class B Amplifier, Class –B Push-pull Amplifier, Complementary Symmetry Class –B Push-pull Amplifier, Distorsion in Power Power Amplifiers, Thermal Stability and Heat Sinks.

Unit- VIII: Tuned Amplifiers Introduction, Q-factor, Small Signal Tuned Amplifiers, Effect of Cascading Single Tuned Amplifiers on Bandwidth Effect of Cascading Double Tuned Amplifiers on Bandwidth, Stagger Tuned Amplifiers, Stability of Tuned Amplifiers.

TEXT BOOKS:

1. INTEGRATED ELECTRONICS – J.MILLIMAN, C.C.HALKIES, 1991 ED, 2008 TMH.

2. ELECTRONIC DEVICES AND CIRCUITS – S.SALIVAHANAN, N.SURESH KUMAR, A.VALLAVARAJ, 2 ED., 2008, TMH

REFERENCES:

1. ELECTRONIC DEVICES AND CIRCUITS – R.L. BOYLESTAD AND LOUIS NASHELSKY, 9 ED., 2006, PEI/PHI.

2. INTRODUCTION TO ELECTRONICS DEVICES AND CIRCUITS – ROBER T. PAYNTER, PE.

3. ELECTRONICS DEVICES AND CIRCUITS – K. LAL KISHORE, 2 ED., 2005. BSP.

4.2 UNIT WISE PLANNER FOR ACADEMIC YEAR 2013 – 2014

Subject: Electronic Circuit Analysis

Unit No.	Date Planned	Date Conducted	Remarks
I			
II			
III			
IV			
V			
VI			
VII			
VIII			

4.3 SESSION PLANNER

S.No	Unit No	Topic	Date Planned	Date Conducted	Remarks
L1		Review, classification of amplifiers			
L2		Distortion in amplifiers			
L3		Analysis of CE Conf. with simplified			
L4		Analysis of CC,CB Conf. with simplified			
L5		Analysis of CE amplifiers with emitter			
L6		Millers Theorem and its dual			
L7		Design of single stage RC Coupled			
		Tutorial			
		Class test			
L8		Analysis of Cascaded RC Coupled BJT			
L9		Cascode Amplifiers			
L10		Darlington pair			
L11		Different Coupling Schemes used in			
L12		RC Coupled Amplifier			
L13		Transformer Coupled Amplifier			
L14		Direct Coupled Amplifier			
		Tutorial			
		Class test			
L15		Lagarithms, Decibles			
L16		General Frequency Considerations			
L17		Frequency response of BJT Amplifier			
L18		Analysis at Low and High Frequencies			
L19		Effect of coupling and bypass Capacitors			
L20		The Hybrid – pi (?) – Common Emitter			
L21		CE Short Circuit Current Gain			
L22		Current Gain with Resistive load			

L23		Single Stage CE Transistor Amplifier			
L24		Gain-Bandwidth Product			
		Tutorial			
		Class test			
L25		Basic concepts, MOS Small signal model			
L26		common source amplifier with Resistive			
L27		Diode connected Load and Current Source			
L28		Source follower			
L29		Common Gate stage Cascode Amplifier			
L30		Folded Cascode Amplifier Frequency			
		Tutorial			
		Class test			
L31		Concept of Feedback, Classification of			
L32		General characteristics of a Negative			
L33		Effect of feedback on Amplifier			
L34		Voltage Series Feedback Configurations			
L35		Voltage Shunt Feedback Configurations			
L36		Current Series Feedback Configurations			
L37		Current Shunt Feedback Configurations			
		Tutorial			
		Class test			
L38		Classification of oscillators, Conditions			
L39		RC Phase Shift Oscillator			
L40		Generalized analysis of LC Oscillators			
L41		Hartley and colpitts Oscillators			
L42		Wien-Bridge Oscillators			
L43		Crystal Oscillators			
L44		Stability of Oscillators.			
		Tutorial			
		Class test			
L45		Classification, Class A Large signal			
L46		Transformer Coupled Class A Audio			
L47		Efficiency of Class A Amplifier			

L48		Class B Amplifier, Efficiency of Class B			
L49		Class –B Push-pull Amplifier			
L50		Complementary Symmetry Class –B			
L51		Distorsion in Power Power Amplifiers			
L52		Thermal Stability and Heat Sinks			
		Tutorial			
		Class test			
L53		Introduction, Q-factor			
L54		Small Signal Tuned Amplifiers			
L55		Effect of Cascading Single Tuned			
L56		Effect of Cascading Double Tuned			
L57		Stagger Tuned Amplifiers			
L58		Stability of Tuned Amplifiers			
		Tutorial			
		Class test			

4.4. QUESTION BANK

4.4.1 UNIT-1

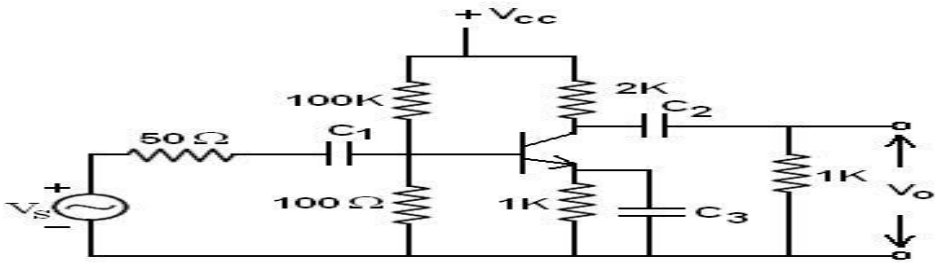
4.4.1.1 DESCRIPTIVE QUESTIONS

1. . (a) A transistor in CB circuit has the following set of 'h' parameters. h_{ib} = 20Ω, h_{fb} = 0.98, $h_{rb} = 3 \times 10^{-4}$, $h_{ob} = 0.5 \times 10^{-6}$. Find the values if R_i, R_o, A_i & A_v if R_S = 600Ω and R_L = 1.5 kΩ.

(b) Draw the CE amplifier with un by passed emitter resistance and derive expression for its R_i & A_v?

2. (a) For a common Emitter configurationcapacitors have negiligible reactance at the test frequency, h_{ie} = 1kΩ, h_{fe} = 99, h_{re} is negligible.

3.(a) For the?circuit shown in figure1, estimate Ai, Av, Ri& Rousing resonable approximations. The h parameters for the transistor are given as hfe= 100, hie= 2kΩ, hre is negligible & hoe= 10−5mhos. **April-2012**



ASSIGNMENT QUESTIONS

1. Draw the simplified hybrid model for the CC circuit and derive expressions for input Resistance, output resistance voltage gain and current gain.

2. Obtain CC 'h' parameters interms of CE parameters

3. For a CE amplifier, calculate the voltage gain, input impedance,output Impedance, current gain. If R_L = 10kΩ, h_{ie} = 1.1kΩ, $h_{re} = 2.5 \times 10^{-4}$, h_{fe} = 50, h_{oe} = 24μA/V.

4.4.1.2 OBJECTIVE QUESTIONS

1. The voltage gain of well designed single stage CB amplifier is essentially determined by ac collector load and

[ ]

A.Emitter resistor R_e B. ac alpha C. Input resistance emitter diode D.ac beta.

2. Typical value of h_{ie} is [ ]

A. 1k B. 25k C.50k D.100k

3. The emitter of a CE amplifier has no AC voltage because of the [ ]
A. DC voltage unit B. Bypass Capacitor C. Coupling capacitor D. load resistance

4. The alpha (α) cut off frequency of a transistor is _____ than is beta (β) cut-off frequency.

5. The parameter h_{22} has units of _____.

6. A CC Amplifier has highest _____but lowest ___

7. The current gain of single stage CE amplifier is nearly equal to_____

8. Which of the following amplifier has high power gain [ ]
(a) CB (b) CE (c) CC (d) both CB and CE

9. The slope of ac load line is _____ that of dc load line. [ ]
(a) same as (b)more than (c) less than (d) None of the above

10. The amplifiers can be classified according to [ ]
(a)frequency range (b)inter stage coupling (c)operation method (d)all the above

11. If Z is the impedance connected between two nodes, node1 and node2, it can be replaced by two separate impedances Z1 and Z2, where Z1 is connected between node1 and ground and Z2 is connected between node2 and ground. This is called _____ theorem. [ ]
(a)Miller (b)Reciprocity (c)Superposition (d)Compensation

12.In Millers theorem the individual impedances Z1 and Z2 are given by _____.

13. When the gain provided by a single stage amplifier is not sufficient, it is to cascade the number of stages of the amplifier. It becomes important to stabilize the voltage amplification of each stage which is not desired. The simple and effective way to obtain voltage gain stabilization is to add _____ to a CE stage.

14. For the emitter follower circuit with R_s=0.5K and R_L=5K, assume h_{fe}=50, h_{ie}=1K, h_{oe}=25μA/V. The current gain is _____.

4.4.1.3 TUTORIAL TOPICS

1.State Miller's Theorem.

2. Derive the expressions for the Voltage gain, input resistance and output resistance of common collector circuit, using simplified Hybrid Model.

3. For a common Emitter configuration, what is the maximum value of R_L for which R_i difers by not more than 10% of its value at $R_L = 0$?

4.4.2 UNIT-II

4.4.2.1 DESCRIPTIVE QUESTIONS

1. (a) Derive the expression for the bandwidth of multistage amplifier

(b) What are the problems of Direct coupled amplifiers?

(c) Why RC coupling is popular?

(d) Why transformer coupling is not used in the initial stage of a multistage amplifier?

2. (a) Explain the Principle of operation of direct coupled amplifier and mention its advantages

(b) What is the use of transformer coupling in the output stage of multi stage amplifier?

(c) Why RC coupling is mostly used for voltage amplifier.

3. (a) Derive the expression for current gain for Darligton pair.

(b) With a neat sketch explain the principle of operation of cascode amplifier and also expressions for its performance measure

ASSIGNMENT QUESTIONS

1. Why RC coupling is mostly used for voltage amplifier.

2. Derive the expression for current gain for Darlington pair.

3. With a neat sketch explain the principle of operation of cascode amplifier and also expressions for its performance measure

4.4.2.2 OBJECTIVE QUESTIONS

1. The most desirable feature of transformer coupling is its [ ]
A.Higher voltage gain B. wide frequency range
C.ability to provide impedance matching D. ability to eliminate hum from the output

2. For matching a circuit of output impedance 200Ω with a load of 8 Ω the turn ratio of the two winding transformer should [ ]
A. 25 B.1/25 C.1/5 D.5

3. Direct coupled amplifiers are especially suited for amplifying extremely _____ frequency signals.

4. The DC resistance of transformer coupling is _____so it is more efficient .

5. The input resistance is good in [ ]
(a)single stage amplifier (b)Darlington connection (c)both a and b (d)Millers circuit

6. It is assumed that R_E=3.3k, h_{ie}=1100,h_{re}=0.25m, h_{fe}=50 and h_{oe}=25μA/V. The input impedance using Darlington connection is [ ]
(a)168.3KΩ (b) 2.5MΩ (c)1.65MΩ (d)190KΩ

7. The different coupling schemes used in amplifiers [ ]
(a)RC coupling (b)Transformer coupling (c)Direct coupling (d)All the above

8. The type of coupled amplifier that is used in radio and TV [ ]
(a)RC coupled amplifier (b)Transformer coupled amplifier
(c)Direct coupled amplifier (d)All the above

9. The input impedance of the circuit can be improved by direct coupling of two stages of emitter follower amplifier. This is called as _____ connection.

10. The darlington pair consists of the following two stages [ ]
(a) CE,CC (b)CE,CB (c)both CE (d) both CC

4.4.2.3 TUTORIAL TOPICS

1. Two BJT CE amplifiers in self biasing configuration are connected in cascade. The following are the parameters of each circuit: The biasing resistors are R1 = 10KΩ; R2 = 5KΩ; Collector resistor Rc = 2KΩ; Emitter Resistor Re=2KΩ. hie=1KΩ; hfe=100. Neglect the effect of hoe. Calculate the Voltage gain, input impedance and output impedance of the above cascade.

2. Explain the Principle of operation of direct coupled amplifier and mention its advantages

3. What is the use of transformer coupling in the output stage of multi stage amplifier?

4.4.3 UNIT-III

4.4.3.1 DESRIPTIVE QUESTIONS

1.Obtain the expressions for the voltage gain in the low frequency, medium frequency and high frequency ranges in the case of single stage amplifier.

2. (a) The hybrid - π parameters of the transistor at room temperature & for I_C = 1.3 mA are g_m = 50 mA/V, $r_{b\,e}$ = 1K, r_{bb} = 100 Ω, $r_{b\,c}$ = 4 MΩ, r_{ce} = 80KΩ, C_C = 3PF & C_e = 100 PF. Using Miller's theorem and the approximate analysis compute the upper

3dB frequency of the current gain and magnitude of the voltage gain at that frequency.

(b) Consider a single - stage CE transistor amplifier with the load resistance R_L shunted by a capacitance C_L. Prove that the internal voltage gain K is

K _ □gmRL

1+j!(CC+CL)RL

3. (a) A transistor amplifier in CE configuration is operating at high frequency with

specifications: f_T = 6 MHz, g_m = 0.04 mhos, h_{fe} = 50, r_{bb} = 100Ω, R_S = 500Ω, C_C = 10 pF, R_L = 100Ω. Compute the voltage gain, upper 3 dB cut of frequency and gain bandwidth product.

(b) Define unity gain frequency. Obtain the necessary relation using transistor frequency response

ASSIGNMENT QUESTIONS

1. A transistor amplifier in CE configuration is operating at high frequency with specifications: f_T = 6 MHz, g_m = 0.04 mhos, h_{fe} = 50, r_{bb} = 100Ω, R_S = 500Ω, C_C = 10 pF, R_L = 100Ω. Compute the voltage gain, upper 3 dB cut of frequency and gain bandwidth product.

2. Define unity gain frequency. Obtain the necessary relation using transistor frequency response.

3. Derive the equation for the lower 3dB frequency of CE configuration

4.4.3.2 OBJECTIVE QUESTIONS

1. The bandwidth of an amplifier can be increased by [ ]
A.decreasing the capacitance of its bypass capacitors B.minimizing the stray capacitance
C.increasing the input signal frequency D. Cascading it
2. Lower cutoff frequency of an amplifier is primarily determined by the [ ]
A.Internal capacitance of the active device
B.Stray capacitance between its wiring and ground
C.ac beta(β) value of its active devices
D.Capacitances of coupling and bypass capacitor
3. The main reason for the variation of amplifier gain with frequency is [ ]
A. the presence of capacitance internal and external B. due to interstage transformation
C. the logarithmic increase in its output power D. miller effect
4. The alpha (α) of the transistor _____ with the increase in frequency.
5. The negative sign of dB gain indicates [ ]
(a)amplification (b)attenuation (c)both a and b (d)boosting
6. Usually the input output characteristics of an amplifier is [ ]
(a)linear (b)parabolic (c)nonlinear (d)exponential

7. Short circuit CE current gain of a transistor is 25 at a frequency of 2MHz if f_β=200KHz. h_{fe} = _____.
8. For the high frequency analysis of BJT _____ model is used.
9. As signal frequencies decrease, the capacitor reactances increase, the current gain _____.
10. Mid frequency gain of a certain amplifier is 100 then voltage gain in dB is _____
11. The bandwidth of a single stage amplifier is ___ that of a multi stage amplifier. [ ]
(a)more than (b) less than (c) same as (d) none

4.4.3.3 TUTORIAL TOPICS

1. Draw the Hybrid-π model for a common emitter transistor and explain
2. 2. Explain about Gain-Bandwidth Product of an amplifier.
3. Draw the hybrid- Π model of common emitter configuration and describe each component in the Π-model.

4.4.4 UNIT-IV

4.4.4.1 DESCRIPTIVE QUESTIONS

1.(a) Draw the FET amplifier equivalent circuit looking into the drain and find its gain & o/p impedance?

(b) Starting with the definition of g_m and r_d, show that if two identical FETs are connected in parallel, g_m is doubled and r_d is halved since $\mu = r_d g_m$, then μ remains unchanged. [8+7]

2.(a) Draw the small signal high frequency equivalent circuit for the source follower and find its voltage gain input and output impedances?

(b) The amplifier stage shown in figure 3 having I_{DSS} = 1mA, V_P = -1V. If the quiescent drain- to - ground voltage is 10V, find R_1?

3. (a) Derive an expression for voltage gain of a common source FET amplifier with and without source resistance included in the circuit.

ASSISNMENT QUESTIONS

1.Why a FET cannot be explained with h-parameters?
2.Derive an expression for Trans - conductance using FET model
3.Draw and explain the FET high frequency model

4.4.4.2 OBJECTIVE QUESTIONS

1. For the operation of enhancement only N- Channel MOSFET, value of gate voltage has to be [ ]
A.High positive B. high negative C. low positive D. zero
2. Class D amplifier uses what type of transistors [ ]
A. JFETs B. BJTs C. MOSFETs D. can use any
3. A MOSFET can be easily destroyed by any _____ on its gate

4. In depletion mode and N- Channel DE MOSFET conducts with V_{gs} is _____.

5**.** The positive gate operation of a N- Channel Depletion MOSFET is known as _____.

6. In the MOS amplifier analysis the main advantage of source follower is [ ]
(a)high input impedance (b)nonlinearity (c)shift dc level (d)driving capability 7. In the MOS amplifiers the advantage of cascade stage [ ]

(a)higher gain (b)higher bandwidth (c)used to build constant current sources (d)all the above

8. In the MOS amplifier, source follower analysis the output resistance is given by _____ .

9. In the MOS amplifiers, the output signal is taken off the source with respect to the ground and the drain is connected directly toV_{DD}. V_{DD} becomes signal ground in the ac equivalent circuit, we have the name common gain. This is also called as _____.

10. A source follower using FET usually has a voltage gain of _____. [ ]
(a) -1 (b) >100 (c) about -10 (d) less than 1 but positive

4.4.4.3 TUTORAIL TOPICS.

1. Derive the expression for the voltage gain of a MOS-Source Follower.

2. Draw and explain the small signal model of a MOS amplifier

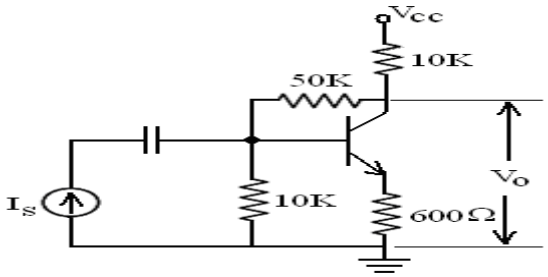
3. The amplifier stage shown in figure 3 having I_{DSS} = 1mA, V_P = -1V. If the quiescent drain- to - ground voltage is 10V, find R_1?

4.4.5 UNIT-V

4.4.5.1 DESCRIPTIVE QUESTIONS

1 a) Derive an expression for the transfer gain of a feedback amplifier.

b)The feedback amplifier shown in figure has transistor parameters



2. (a) Discuss about the types of negative feedback amplifiers giving the effect of each type of feedback on the parameters of the amplifier.

(b) What sort of feedback is employed in a CE amplifier with unbypassed emitter resistor? Discuss its analysis in detail.

3. (a) What are the characteristics of an amplifier that are modified by negativefeedback?

(b) Draw the four types of feedback amplifiers naming them.

(c) Define sensitivity & Desensitivity factors in feedback Amplifiers.

ASSIGNMENT QUESTIONS

1. Explain and justify the effect of Nagative feed back on the characteristics of an amplifier.

2. An amplifier with open loop gain of 2000±150 is available. It is necessary to have the amplifier whose voltage gain varies by not more than ±0.2%. Calculate the feedback factor β, and the gain of the amplifier with feedback.

3. What sort of feedback is employed in a CE amplifier with unbypassed emitter resistor? Discuss its analysis in detail.

4. Describe with aid of suitable diagram, the principal method of SSB power generation

4.4.5.2 OBJECTIVE QUESTIONS

1. Negative feedback in amplifier [ ]
(a) improves SNR at the input (b) improves SNR at the output

(c) Increases distortion (d) None of the above

2. The gain of an amplifier with feedback is _____. [ ]
(a) A/1+Aβ (b) β/1+βa (c) β/1-βa (d) A/1-Aβ

3. The Trans conductance amplifier is also called as _____.

4. In an ideal voltage amplifier, the values of R_i & R_0 are _____.

5. The ratio of input impedance with feedback to without feedback is _____.

6. The disadvantage of negative feedback is [ ]
(a)gain decreases (b)gain is always zero (c)gain is undefined (d)gain increases

7. With series feedback, (voltage or current), input resistance of an amplifier [ ]
(a)decreases (b)increases (c)zero (d)infinity

8. Characteristics of an ideal voltage amplifier are: [ ] (a)A_V=infinity (b)Ri=infinity (c)Ro=0 (d)All the above

9. βA in feedback amplifier circuits is called _____.

10. In the case of voltage shunt feedback amplifier, expression for input impedance with feedback is Zif = _____

4.4.5.3 TUTORIAL TOPICS

1. What are the characteristics of an amplifier that are modified by negative feedback?

2. Draw the four types of feedback amplifiers naming them.

3. Define sensitivity & Desensitivity factors in feedback Amplifiers.

4.4.6 UNIT-VI

4.4.6.1 DESCRIPTIVE QUESTIONS

1. (a) Derive an expression for frequency of oscillation of a RC phase-shift oscillator using a FET.

(b) In a Hartley oscillator L 2 = 0.04 mH and C = 0.004 µF. If the frequency of oscillation is 150 KHz, find . Neglect mutual inductance.

2. Design a RC phase-shift oscillator to operate at a frequency of 5KHz. use a MOSFET with _ = 55 and rd = 5.5K. The phase - shift network not load the amplifier.

(a) Find the minimum value of the drain - circuit resistance for which the circuit will oscillate.

(b) Choose reasonable values of R and find C.

3. Draw the Electrical model of a piezoelectric crystal.

(b) Sketch the reactance Vs frequency function.

(c) Over what portion of the reactance curve do we desire oscillations to take place when the crystal is used as part of a sinusoidal oscillator? Explain.

4. (a) Sketch a circuit of a crystal - controlled oscillator and explain its function.

(b) Explain the frequency - stability criterion for a sinusoidal oscillator.

.

ASSIGNMENT QUESTIONS

1. Derive the expression for the frequency of oscillations of a BJT-RC Phase shift Oscillator.

2. Sketch a circuit of a crystal - controlled oscillator and explain its function

3. Explain the frequency - stability criterion for a sinusoidal oscillator

4.4.6.2 OBJECTIVE QUESTIONS

1. For generating a sinusoidal wave of 1KHz frequency, the most suitable oscillator is __ [ ]

(a) Hartley (b) Colpitts (c) Wien bridge (d) None of the above

2. The frequency stability of LC oscillator is _____ than RC oscil [ ]

(a) less (b) more (c) either a or b (d) None of the above

3. An important limitation of a crystal oscillator is _____. [ ]

(a) its low output (b) its high Q (c) less availability of quartz crystal (d) its high output

4. An oscillator using LC tuned circuit has L= 58.6μH & C=300pF, then the frequency of oscillations will be _____.

5. In a RC phase shift oscillator, each RC section provides a phase shift of _____.

6. Oscillator circuits employ _____ type of feed back [ ]
(a)positive (b)no feed back (c)negative (d)none

7. The range of frequencies over which RC phase shift oscillator circuit is used is _____.

8. In the feedback network if two inductors and one capacitor elements are used the oscillator circuit is called _____ oscillator.

9. In the case of Collpitts oscillator frequency fo= _____ .

10. Expression for frequency of oscillations in the case of Wien Bridge Oscillator is _____.

a. 32KHZ b. 10KHZ c. 20KHZ d. 15KHZ

4.4.6.3 TUTORIAL TOPICS

1. Design a RC phase-shift oscillator to operate at a frequency of 5KHz. use a MOSFET with μ = 55 and rd = 5.5K. The phase - shift network not load the amplifier.

(a) Find the minimum value of the drain - circuit resistance for which the circuit will oscillate.

(b) Choose reasonable values of R and find C.

2.Draw the Electrical model of a piezoelectric crystal.

3. Sketch the reactance Vs frequency function

4.4.7 UNIT-VII

4.4.7.1 DESCRIPTIVE QUESTIONS

1.(a) What is push-pull configuration and how does this circuit reduce the harmonic distortion?

(b) For a class B amplifier providing a 20V peak signal to a 16 load operates on a power supply of Vcc = 30V. Determine the input power, output power and circuit efficiency.

2. (a) Derive an expression for the output power of a class A large - signal amplifier in terms of Vmax Vmin Imax & Imin.

(b) For a particular power amplifier, the optimum load impedance is 180. Calculate the turns ratio required to match an 8 load to this transistor. If the amplifier takes a mean collector current of 2A from a 15V supply and delivers an ac load power of 2.5W to the transformer coupled - load, calculate the

efficiency and the collector dissipation(neglecting the losses)

3. (a) What is a class B amplifier? Where is it employed? Give its circuits, design equations, characteristics & limitations.

(b) A transformer coupled class A large signal amplifier has maximum and minimum values of collector to emitter voltage of 25V and 2.5V. Determine its collector efficiency.

4. (a) A transistor supplies 0.8W to a 5K load. The zero signal dc collector current is 30mA, and the dc collector current with signal is 36mA. Determine the percent second - harmonic distortion.

(b) Define conversion efficiency. Determine the maximum value of conversion efficiency for a series - fed class A power amplifier.

ASSIGNMENT QUESTIONS

1. Describe the circuit of an FET amplitude limiter, and with the aid of the transfer Characteristic explain the operation of the circuit.

2. What can be done to improve the overall limiting performance of an FM receiver? Explain the operation of the double limiter and also AGC in addition to a limier.

3. List out the consequences of choosing the IF very high or very low.

4. Present the differences between AM and FM receivers.

4.4.7.2 OBJECTIVE QUESTIONS

1. With transformer connection to load the maximum efficiency of the class A amplifier will go up to a maximum of [ ]

a. 78.5% b.25% c.50% d.66%

2. In ____ power amplifier, the output signal varies for a full 360^0 of the cycle. [ ]
(a)Class A (b) Class B (c) Class AB (d) None of the above

3. Maximum theoretical efficiency of Class B push pull amplifier is ___. [ ]

(a)25.5% (b) 50% (c) 75% (d) 78.5%

4. Thermal resistance of the heat sink will be typically _____.

5. If output power=20W and the input dc power=60W,then the efficiency of power amplifier is _____. 6. In Class B power amplifier, Q-point is set _____ .

7. In class B amplifiers relation between maximum power dissipation Pc and maximum output power dissipation Po is Pc= ____ Po [ ]
(a)0.1 (b)0.2 (c)0.3 (d)0.4

8. Due to input signal swing, if the operating point shifts into cutoff and saturation regions, that amplifier is classified as _____ amplifier. [ ]
(a)small signal (b)large signal (c)both a and b (d)not an amplifier

9. The coupling employed in amplifier circuits are [ ]
(a)RC coupling (b)Transformer coupling (c)LC tuned coupling (d)All the above
10. Due to input signal swing, if the operating point shifts into cutoff and saturation regions, that amplifier is classified as _____ amplifier [ ]
(a)small signal (b)large signal (c)both a and b (d)not an amplifier
11. The maximum theoretical efficiency of class B push pull amplifier is _____.
12. Maximum efficiency of transformer coupled amplifiers is _____ .

4.4.7.3 TUTORIAL TOPICS

1. Derive the expression for the efficiency of a direct coupled Class-A amplifier.

2. What is crossover distortion? Explain.

3.What is push-pull configuration and how does this circuit reduce the harmonic distortion?

4.4.8 UNIT-VIII

4.4.8.1 DESCRIPTIVE QUESTIONS

1. (a) Draw the equivalent circuit of a double tuned amplifier and derive the expression for gain at resonance.

(b) Derive the expression for effective bandwidth of cascaded tuned amplifier.

2. (a) Draw the equivalent circuit of a single tuned capacitive coupled amplifier and derive the expression for gain at resonance.

(b) Draw the circuit diagram for tuned RF amplifier and explain its working.

3. (a) Draw the frequency response of tapped single tuned capacitance coupled amplifier and derive the expression for L for maximum power transfer.

(b) Draw the circuit of double tuned amplifier and explain its working.

4. (a) Compare neutralization and unilaterlisation methods of tuned amplifiers.

(b) What are the limitations of stagger tuned amplifiers?

(c) What happens when no. of stages is increased in single tuned cascaded amplifiers?

ASSIGNMENT QUESTIONS

1. Write notes on Stagger Tuning

2. Single Tuned and Double Tuned Amplifiers.

3. Draw the equivalent circuit of a single tuned capacitive coupled amplifier and derive the expression for gain at resonance.

4.4.8.2 OBJECTIVE QUESTIONS

1. In tuned amplifiers, harmonic distortion is _____. [ ]
(a) infinite (b) more (c) less (d) None
2. Double tuned amplifier provides ____ bandwidth than single tuned amplifiers.[ ]
(a)larger (b) smaller (c) negligible (d)constant

3. Tuned amplifiers can be used in _____. [ ]

(a)Radar (b)IF amplifiers (c) both a and b (d)None
4.Small signal tuned amplifiers are operated in _____ mode.
5. Parallel tuned circuit is also known as _____.
6. The application of Tuned amplifier is [ ]
(a)radio signals (b)RF amplifier (c)Communication receivers (d)All the above
7. The purpose of resonant circuits in tuned circuits is [ ]
(a)provide properly matching load impedance (b)reset unwanted harmonics
(c)couple power to load (d)all the above

8. Double tuned amplifier provides _____ band width than single tuned amplifier.[]
(a) smaller (b)larger (c)equal (d)zero
9. Two resonant circuits tuned to different frequencies is called _____ tuning.
10. In tuned amplifiers equivalent circuits, the model used for transistor is _____.

4.4.8.3 TUTORIAL TOPICS

1. Draw the equivalent circuit of a single tuned capacitive coupled amplifier and derive the expression for gain at resonance.

2. Draw the circuit diagram for tuned RF amplifier and explain its working.

3.Compare neutralisation and unilaterlisation methods of tuned amplifiers.

5. PULSE AND DIGITAL CIRCUITS

5.1 JNTUH SYLLABUS

UNIT I

LINEAR WAVESHAPING : High pass, low pass RC circuits, their response for sinusoidal, step, pulse, square and ramp inputs. RC network as differentiator and integrator, attenuators, its applications in CRO probe, RL an RLC circuits and their response for step input, Ringing circuit.

UNIT II

NON-LINEAR WAVE SHAPING : Diode clippers, Transistor clippers, clipping at two independent levels, comparators, applications of voltage comparators, clamping operation, clamping circuits taking source and diode resistance into account, Clamping circuit theorem, practical clamping circuits, effect of diode characteristics on clamping voltage, Synchronized Clamping.

UNIT III

SWITCHING CHARACTERISTICS OF DEVICES : Diode as a switch, piecewise linear diode characteristics, Diode switching times,Transistor as a switch, Break down voltages,transistor in saturation,Temperature variation of saturation parameters, transistor-switching times,Silicon controlled-switch circuits.

UNIT IV

MULTIVIBRATORS : Analysis and Design of Bistable, Monostable, Astable Multivibrators and Schmitt trigger using transistors.

UNIT V

TIME BASE GENERATORS : General features of a time base signal, methods of generating time base waveform, Miller and Bootstrap time base generators – basic principles, Transistor miller time base generator, Transistor current time base generator,methods of Linearioty improvement.

UNIT VI

SAMPLING GATES : Basic operating principles of sampling gates, Unidirectional and Bi-directional Sampling gates,four diode sampling gates, Reduction of pedestal in gate circuits, six Diode gate, Applications of sampling gates.

UNIT VII

SYNCHRONIZATION AND FREQUENCY DIVISION : Pulse synchronization of Relaxation devices,Frequency, Frequency division in sweep circuit,Stability of Relaxation devices, Astable relaxation circuits, Monostable relaxation circuits, Synchronization of a sweep circuit with symmetrical signals, Sine wave frequency division with a sweep circuit. A Sinusoidal divider using Regeneration and Modution.

UNIT VIII

REALIZATION OF LOGIC GATES USING DIODES & TRANSISTORS : AND, OR and NOT gates using Diodes and Transistors,DCTL,RTL,DTL,TTL AND CML Logic Families and its comparision..

TEXT BOOKS :

1. Pulse, Digital and Switching Waveforms - J. Millman and H. Taub, McGraw-Hill, 1991.

2. Solid State Pulse circuits - David A. Bell, PHI, 4th Edn., 2002 .

REFERENCES :

1. Pulse and Digital Circuits – A. Anand Kumar, PHI, 2005.

2. Wave Generation and Shaping - L. Strauss.

3. Pulse, Digital Circuits and Computer Fundamentals - R.Venkataraman

5.2 UNIT WISE PLANNER FOR ACADEMIC YEAR 2013 - 2014

Subject: Pulse and Digital Circuits

Unit No.	Date Planned	Date Conducted	Remarks
I			
II			
III			
IV			
V			
VI			
VII			
VIII			

5.3 SESSION PLANNER

S.No	Unit No	Topic	Date Planned	Date Conducted	Remarks
1	I	High pass, low pass RC circuits			
2		Sinusoidal response			
3		Step response			
4		Pulse response			
5		Square response			
6		Ramp response			
7		RC network as differentiator			
8		RC network as integrator			
9		Attenuators, its applications in CRO probe			
10		RLC Series circuits			
11		RLC Parallel circuits			
12		Ringing circuit			
13	II	Diode clippers			
14		Transistor clippers			
15		clipping at two independent levels			
16		Comparators, applications of voltage comparators			
17		clamping operation			
18		clamping circuits taking source and diode resistance into account			
19		Clamping circuit theorem			
20		practical clamping circuits			
21		effect of diode characteristics on clamping voltage			
22		Synchronized Clamping			
23		Diode as a switch			
24		piecewise linear diode characteristics			
25		Diode switching times, Transistor as a switch			

26	III	Break down voltages, transistor in saturation			
27		Temperature variation of saturation parameters			
28		transistor-switching times, Silicon controlled-switch circuits			
29	IV	Analysis and Design of Bitable,			
30		Monostable			
31		Astable Multivibrators			
32		Schmitt trigger using transistors.			
33		Revision			
34	V	General features of a time base signal			
35		methods of generating time base waveform			
36		Miller and Bootstrap time base generators			
37		Miller and Bootstrap time base generators			
38		Transistor miller time base generator,			
39		Transistor current time base generator			
40		methods of Linearity improvement			
41		Revision			
42	VI	Basic operating principles of sampling gates			
43		Unidirectional Sampling gates			
44		Bi-directional Sampling gates			
45		four diode sampling gates			
46		Reduction of pedestal in gate circuits			
47		six Diode gate			
48		Applications of sampling gates			
49		Revision			
50	VII	Pulse synchronization of Relaxation devices			
51		Frequency division in sweep circuit			
52		Stability of Relaxation devices			
53		Astable relaxation circuits			
54		Monostable relaxation circuits			
55		Synchronization of a sweep circuit with symmetrical signals			

56		Sine wave frequency division with a sweep circuit			
57		A Sinusoidal divider using Regeneration and Modulation			
58	VIII	AND, OR and NOT gates using Diodes ..			
59		AND, OR and NOT gates using Transistors			
60	VIII	DCTL,RTL			
61		DTL,TTL			
62		CML Logic Families			
63		Comparison of logic families			
64		Revision			

5.4. QUESTION BANK

5.4.1 UNIT-1

5.4.1.1. DESCRIPTIVE QUESTIONS

1. (a) Prove that an RC circuit behaves as a reasonably good integrator if RC > 15T, Where T is the period of an input 'Em sin ωt'.

(b) What is the ratio of the rise time of the three sections in cascade to the rise time of Single section of low pass RC circuit.

2. (a) Verify V2= (V/2)(e2x−1)/(e2x+1) = (V/2) tanhx for a symmetrical square wave applied to a low pass RC circuit.

(b) Derive the expression for percentage tilt(P) of a square wave output of RC high pass circuit.

3. (a) What is the function of a comparator? Explain its operation.

(b) Explain the response of a low pass circuit to an exponential input is applied.

(c) Explain the response of RL circuit when a rectangular pulse is applied

4. (a) Derive the expression for rise time of integrating circuit and prove that it is proportional to time constant and inversely proportional to upper 3 dB frequency.

(b) Explain the operation of RC low pass circuit for exponential input is applied.

5. (a) A square wave whose peak-to-peak value is 1V, extends ±0.5V with reference to ground. The half period is 0.1 sec This voltage impressed upon an R.C. differentiating circuit whose time constant is 0.2 sec. Determine the maximum and minimum values of the output voltage in the steady state.

(b) Draw the response of high pass circuit for square wave and derive the expression for percentage tilt.

6. Wtite short note on the following:

(a) Attenuators

(b) RC Double differentiator.

(c) RLC ringing circuit.

7. Derive an expression for the percentage tilt of the output of a high-pass RC circuit with large time constant excited by a symmetrical square wave with zero average value.

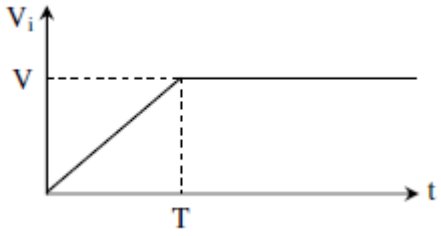
(b) A square wave whose peak-to-peak amplitude is 2V extends ± IV with respect to ground. The duration of the positive section is 0.1 sec and that of the negative section 0.2 sec. If this waveform is impressed upon an RC integrating circuit whose time constant is 0.2 sec, What are the steady – state maximum and minimum values of the output waveform?

8. (a) Derive an expression for the output of a high-pass circuit excited by an exponential input.

(b) A square-wave whose peak-to-peak value is 1 V extends ± 0.5 V with respect to ground. The duration of the positive section is 0.1 sec and of the negative section0.2 sec.If this waveform is impressed upon an RC differentiating circuit whose time constant is 0.2sec, what are the steady – state maximum and minimum values of the output waveform?

9. (a) Prove that the high pass and low pass RC circuits act as differentiator and Integrator respectively.

(b) The limited ramp shown in figure is applied to an RC differentiator. Draw the output waveforms for the cases (a) T = 0.2 RC (b) T = RC and (C) T = 5RC.



10. (a) Why does a resistive attenuator need to be compensated? Explain different methods of ompensation. What is the effect of the output resistance of the generator on an attenuator output?

(b) A square wave whose peak-to-peak amplitude is 1 V extends ±0.5V with respect to ground. The duration of the positive section is 0.2 sec and that of the negative section is 0.3 sec. If this waveform is impressed upon an RC integrating circuit whose time constant is 0.3 sec, What are the steady-state maximum and minimum values of the output waveform?

ASSIGNMENT QUESTIONS

1. Derive the relation between rise time and bandwidth of low pass RC circuit

2. Derive the expression for percentage tilt (p) of a square wave output of RC high pass circuit

5.4.1.2 OBJECTIVE QUESTIONS

1. Except for the sinusoidal signal, no other signal can preserve its when the transmitted through a [ ]

a) Linear network b) Passive network c) Both d) None

2. The process where by the form of non sinusoidal signal is altered by transmission through a linear network is called[ ]

a) Non linear wave shaping b) linear wave shaping c) Both d) None

3. The low pass circuit [ ]

a) allows low frequencies, rejects high frequencies b) Allows all frequencies

c) Allows high frequencies d) None

4. The high pass circuit [ ]

a) Allows low frequencies b) Allows high frequencies, rejects low frequencies

c) Allows all frequencies d) None

5. The Low pass filter acts as [ ]

a) Integrator b) Differentiator c) Both d) None

6. The high pass filter acts as [ ]

a) Integrator b) Differentiator c) Both d) None

7. The Upper cut off frequency of LPF equals to [ ]

a) Bandwidth b) Lower cut off frequency c) Both d) None

8. The Upper cut off frequency of LPF equals to [ ]

a) 1 / RC b)1 / 2лRC c)1 / 2.2 RC d) None

9. The time taken by output waveform to rise from 10% to 90% is [ ]

a) Rise time b) Tilt timec) Transition Time d) None

10. The frequency at which the gain is 1 / $\sqrt{2}$ times of its maximum value is called [ ]

a) Cut off frequency b) maximum frequency c) Minimum frequency d) None

11. Which are preferred in analog computers [ ]

a) Integrator b) Differentiator c) Both d) None

12. For a perfectly compensated attenuator [ ]

a)$V_o(0^+)$=Vo(∞) b) $V_o(0^+)$>Vo(∞) c) Both d) None

13. For an over compensated attenuator [ ]

a)$V_o(0^+)$>Vo(∞) b) $V_o(0^+)$<Vo(∞) c) Both d) None

14. For a un damped attenuator [ ]

a)$V_o(0^+)$>Vo(∞) b) $V_o(0^+)$<Vo(∞) c) Both d) None

15. The process of converting pulses into pips by means of a circuit of very short time constant is called [ ]

a) Peaking b) Ringing c) wave shaping d) None

16. The high pass RC circuit is called as [ ]

a) Capacitive coupling network b) Inductive coupling network c) Both d) None

17. The high pass circuit very small time constant is called [ ]

a) Ringing b) Peaking c) wave shaping d) None

18. The upper cut off frequency of HPF is [ ]

a) Infinity b) Finite c) Low d) High

19. The bandwidth of HPF is [ ]

a) Infinity b) Finite c) Low d) High

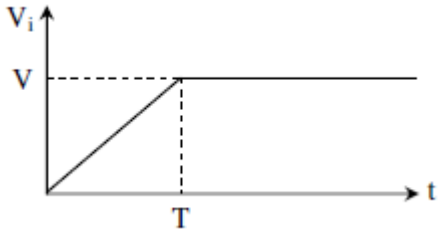
20. A High pass circuit is treated as a differentiator, if the phase shift between the input and output is at least [ ]

a) 89.4^0 b) 90^0 c)180^0 d) None

5.4.1.3 TUTORIAL TOPICS

1 A square wave whose peak-to-peak value is 1V, extends ±0.5V with reference to ground. The half period is 0.1 sec This voltage impressed upon an R.C. differentiating circuit whose time constant is 0.2 sec. Determine the maximum and minimum values of the output voltage in the steady state.

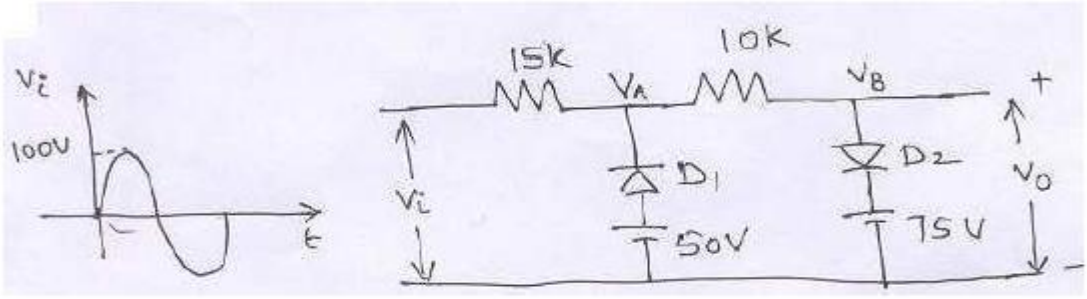
2 The limited ramp shown in figure is applied to an RC differentiator. Draw the output waveforms for the cases (a) T = 0.2 RC (b) T = RC and (C) T = 5RC.



5.4.2 UNIT-II

5.4.2.1 DESCRIPTIVE QUESTIONS

1. (a) For the circuit shown in figure 2a , V_i is a sinusoidal voltage of peak 100 volts. Assume ideal diodes. Sketch one cycle of output voltage. Determine the maximum diode Current.



(b) Explain positive peak clipping with reference voltage.

2. (a) Draw the circuit diagram of slicer circuit using Zener diodes and explain its operation with the help of its transfer characteristic.

(b) Draw the circuit diagram of emitter coupled clipper. Draw its transfer characteristics indicating all intercepts, slopes and voltage levels derive the necessary equations.

3. (a) State and prove clamping -circuit theorem.

(b) A clamping circuit and input wave form is shown in figure 2b calculate and

plot to scale the steady state output

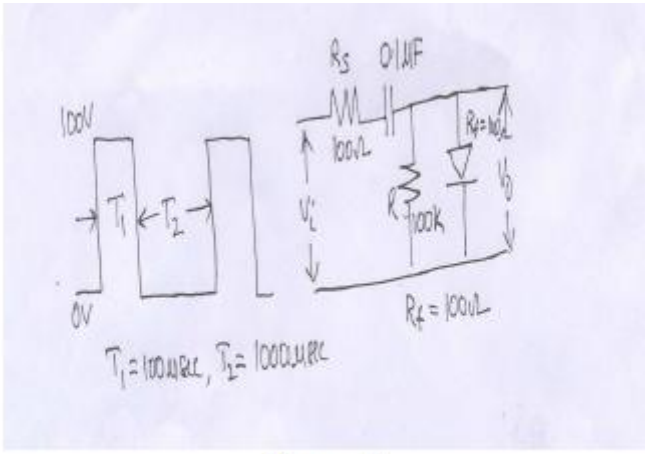


Figure 2b

4. (a) Give the circuits of different types of shunt clippers and explain their operation with the help of their transfer characteristics.

(b) Draw the diode differentiator comparator circuit and explain the operation of it when ramp input signal is applied.

5. (a) T=1000 μ sec

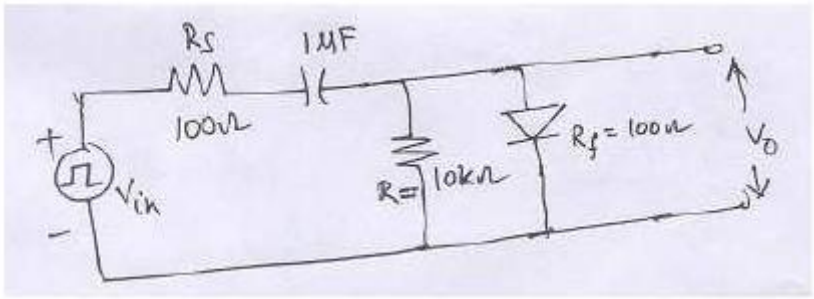
V= 10 V

Duty cycle = 0.2

i. Sketch waveform with voltage levels at steady state figure 2(a)iii

ii. Forward and reverse direction tilt

iii. A_f / A_r



(b) Write a short note on non- linear wave shaping.

6. (a) For the circuit shown in figure 2a Vs is a sinusoidal voltage of peak 75 volts. Assuming ideal diodes. Sketch one cycle of output voltage. Determine the maximum diode currents.

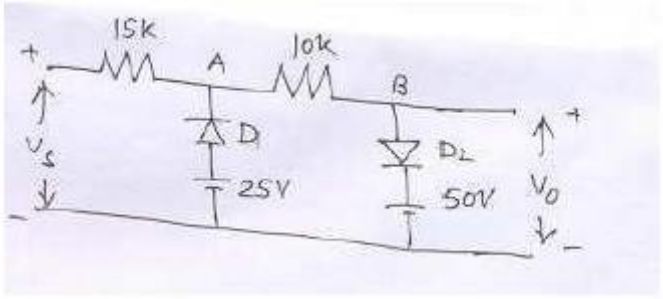


Figure 2a

(b) What are the uses of clipper circuits.

7. (a) A symmetrical 10 kHz square wave whose peak -to-peak excursion are ±10V with respect to ground is impressed upon the diode clamping circuit shown in figure 2a. The Diodes has R_f = 100 , R_r = α and V = 0. Sketch the steady state output waveform Indicating clearly the voltage levels.

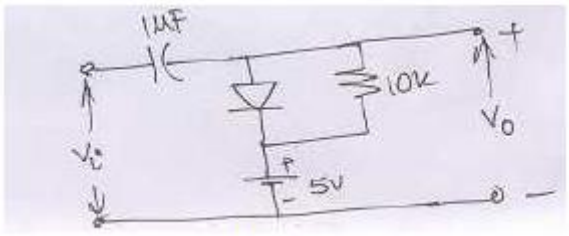


Figure 2a

(b) Explain positive peak voltage limiters above and below reference level.

8. (a) For the circuit shown in figure 2a an input voltage V_i linearly from 0 to 150V is applied. Sketch the output waveform V_0 to the same time scale. Assume ideal diodes.

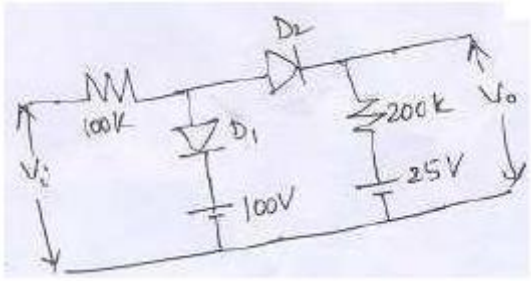
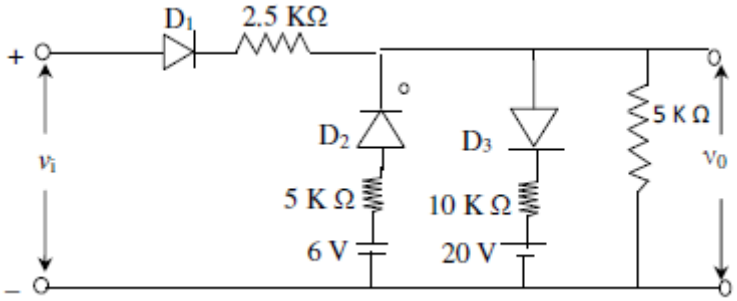


Figure 2a

(b) What in meant by a d.c restoration circuit and explain?

9. (a) State and prove clamping circuit theorem

(b) For the clipping circuit shown in fig. make a plot of _0 versus _i for the range of _i from 0 to 50 V. indicate all slopes and voltage levels. Also, indicate for each region, the diodes which conduct.



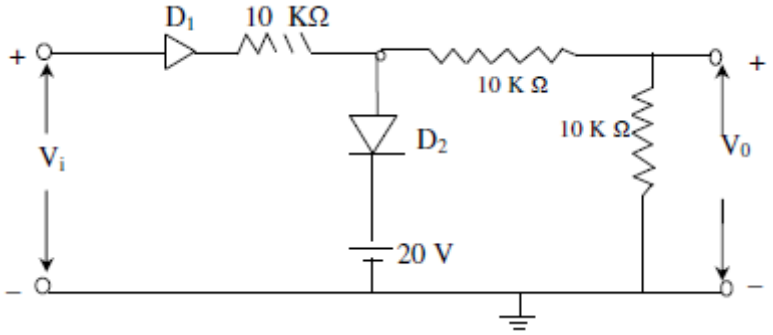
10. (a) With the help of a neat circuit diagram, explain the working of a two- level diode clipper. Write the transfer characteristic equations and plot the curve.

(b) In the clamping circuit, $R_s = R_f = 50\ \Omega$, $R = 20\ k\Omega$ and $e = 2\ \mu F$. A Symmetrical square wave signal of amplitude 20V and frequency 5 KHz is applied at t=0. Draw the first three cycles of the output waveform.

11. (a) With the help of neat circuit diagram and wave forms, explain the working of a transistor clipper.

(b) A symmetrical 10 K Hz square wave whose peak - to – peak excursions are ± 10 V with respect to ground is impressed on the clamping circuit. Here R = 10 K_, C = 1 μ F, the diode has $R_r = \Omega$, $R_f = 0$, $V_r = 0$ and the source impedance R_s is zero. (i) Sketch the output waveform. (ii) If the diode forward resistance is1k_, sketch the output waveform. Calculate the maximum and minimum values with aspect to ground. (iii) Repeat part (ii) if the source impedance is 1k

12. (a) For the circuit shown in fig., Plot V_o uessus V_i indicating all intercepts, slopes and voltages levels, if V_i varies linearly from 0 to 50 V.



(b) In the clamping circuit, $R_s = 100\ \Omega$, $R_f = 50\ \Omega$ $R = 100K\Omega$ and $e = 2\ \mu F$. A symmetrical square wave signal of amplitude 20V and frequency 5KHz is applied at t=0. Draw the first three cycles of the output waveform.

ASSIGNMENT QUESTIONS

1 State and prove clamping circuit theorem with diagrams

2 Draw and explain emitter coupled clipper

5.4.2.2 OBJECTIVE QUESTIONS

1 Clipping circuits are used to [ ]

a)reject the signal b)amplify the signal c)remove the part of the signal d)none

2 The circuits which are used to select for transmission a part of the waveform are called [ ]

a)clipping circuits b)clamping circuits c)linear wave shaping d)none

3 Clipping circuits are referred as [ ]

a)slicers b)current limiters c)voltage limiters d)all

4 In a_____ when the diode is on, the output follows the input [ ]

a)series diode clipper b)shunt diode clipper c)comparator d)none

5 The external resistance R in a series or shunt clipper is given by [ ]

a) $R=R_r$ b) $R=\sqrt{R_r/R_f}$ c)) $R=\sqrt{R_rR_f}$ d)none

6. In clipping circuits the capacitors are [ ]

a) Un avoidable b) desirable c) essential d) None

7 The diode used in a clipping circuit, has $R_f = 25\Omega$, $R_r = 1M\ \Omega$. The external resistance R = [ ]

a) 50K Ω b) 5K Ω c) 100K Ω d) None

8. A shunt diode clipper is required to clip off the input which is exactly above 4.6V. The diode has V_r=0.6V the value of V_R must be [ ]

a) 4V b)8V c) 15V d) None

9. A Diode has $R_f = 10\Omega$, $R_r = 100K\ \Omega$ its figure of merit is [ ]

a) 10000 b)10 c) 100 d)None

10. A Wave form which is above 6V and below -4V is to be clipped off properly. The diode has V_r=0.6V. The reference voltage sources to be used are [ ]

a) 5.4V & -3.4V b) 5.5V & -3.4V c) 6.3V & 3.3V d) None

11. A metal semiconductor diode is also called [ ]

a) PN – Diode b) Hot Carrier Diode c) Cold carrier diode d) None

12. In a _____ when the diode is off, the output follows the input [ ]

a) Series diode clipper b) Shunt diode clipper c) comparator d)none

13. A Transistor has [ ]

a) No Non- Linearity b) one-non-linearity c) Two non-linearties d) None

14. When the emitters of two identical transistors are coupled we get [ ]

a) Single ended clipper b) double ended clipper c) Coupled clipper d) None

15 The circuit is used to mark the instant when an arbitary wave form attains some reference level is called

a)marker b)comparator c) Both d) None

16 Regenerative comparators employ [ ]

a) Clipping circuits b) Clamping circuits c) Schmitt Trigger d) None

17. A circuit which restores or reinserts the last dc component is called [ ]

a) clipping circuit b) Clamping circuits c) Schmitt Trigger d) None

18. A circuit which clamps the positive peak of a signal to zero level is called [ ]

a) +ve Clamping Circuitb) -ve Clamping Circuit c) +ve Peak Clamping d) none

19. In a +ve Clamping the entire input wave form appears [ ]

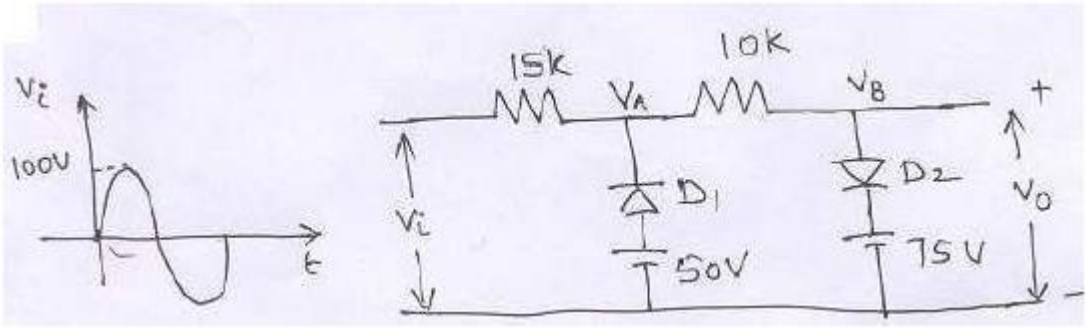
a) above ref. level b) below ref. level c) Symmetrically w.r.t ref. levels d) none

20. Non linear wave shaping circuits are [ ]

a) clipping circuit b) Clamping circuits c) both d) None

5.4.2.3 TUTORIAL TOPICS

1. For the circuit shown in figure 2a , V_i is a sinusoidal voltage of peak 100 volts. Assume ideal diodes. Sketch one cycle of output voltage. Determine the maximum diode Current.



2 A clamping circuit and input wave form is shown in figure 2b calculate and plot to scale the steady state output

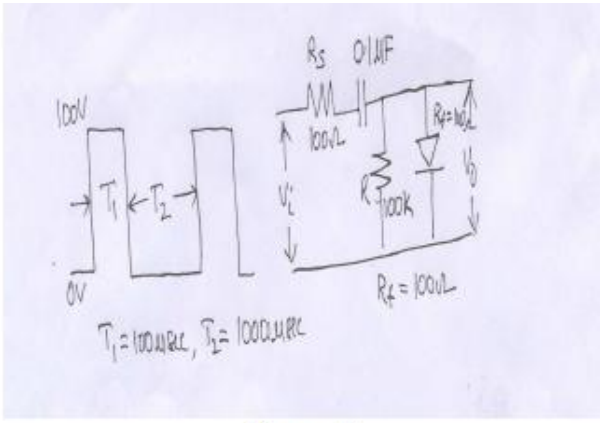


Figure 2b

5.4.3 UNIT-III

5.4.3.1 DESCRIPTIVE QUESTIONS

1. (a) Explain the terms pertaining to transistor switching characteristics.

i. Rise time. ii. Delay time. iii. Turn-on time. iv. Storage time. v. Fall time. vi. Turn-off time.

(b) Give the expression for risetime and falltime in terms of transistor parameters and operating currents.

2. Write Short notes on:

(a) Diode switching times (b) Switching characteristics of transistors (c) FET as a switch.

3. (a) Explain the behaviour of a BJT as a switch in electronic circuits. Give an example.

(b) Write a short note on the switching times of transistor.

4. (a) Sketch neatly the waveforms of current & voltages for a transistor switch with capacitance loading circuit.

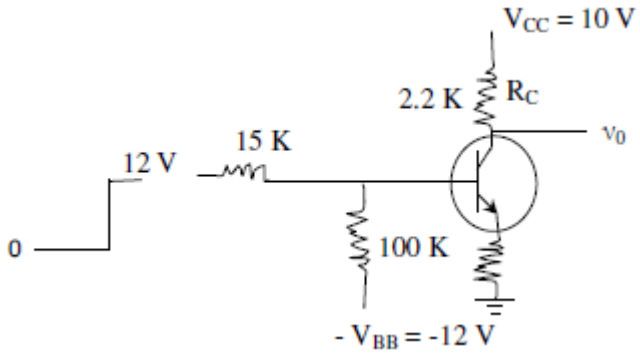
(b) What are catching diodes?

(c) Design a transistor switch, with the following data. V_{CC} = 10 V; V_{BB} = 6 V; $I_{C\,sat}$ = 10 mA, $(hFE)_{min}$ = 30,

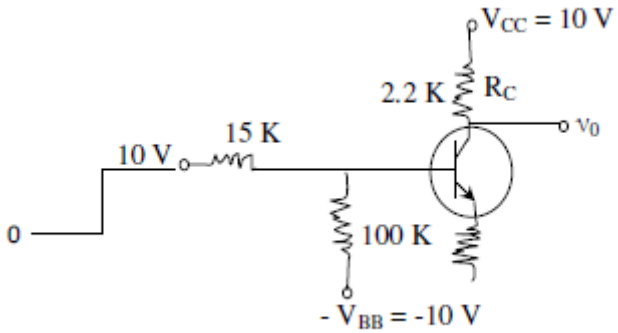
Given NPN silicon transistor with negligible I_{CBO}. Assume junction voltages.

5. (a) Briefly discuss the switching times of a junction diode.

(b) Show that the circuit given below works as a switch. Assume junction voltages and $(h_{FE})_{min}$ = 30.



6. Prove that the circuit show works as a transistor switch. Assume junction voltage and $(h_{FE})_{min}$ = 30.



ASSIGNMENT QUESTIONS

1 Explain the terms pertaining to transistor switching characteristics

(a)Rise time (b)Delay time (c)Turn-on time (d)Storage time (e)Fall time (f)Turn-off time

5.4.3.2 OBJECTIVE QUESTIONS

1.A transistor acts as an open switch when it is in [ ]

a) Cut –off b) Active c) Saturation d. none

2. A transistor acts as a closed switch when it is in [ ]

a) Cut –off b) Active c) Saturation d. none

3. For a transistor to be in saturation [ ]

a) both junctions must be forward biased b) both junctions must be reverse biased c) both d) none

4. For a transistor to be in cut –off region both junctions of the transistor must be[ ]

a) forward biased b) reverse biased c) Un – Biased d) none

5. For a transistor to be in the active region [ ]

a) both junctions must be forward biased b) both junctions must be reverse biased

c) emitter base junction must be reverse biased and collector base junction must be forward biased

d) emitter base junction must be forward biased and collector base junction must be reverse biased

6. A transistor acts as an amplifier when it is [ ]

a) Saturation b) Active C) Cut – Off d) None

7. The break down which occurs through a direct rupture of the bonds because of the existence of the strong electric field referred to as[ ]

a) Zener Break Down b) Avalanche break down c) both d) none

8. In the steady state condition the current which flows through a diode is a [ ]

a) diffusion current b) Drift current c) both d) None

9. The reverse saturation current doubles for every_____ rise in temperature[ ]

a) 100^0 C b) 10^0 C c) 1^0 C d) none

10. A 6V1 Zener break down occurs below [ ]

a) 6V1 b) 9V1 c) 3V1 d) None

11. The capacitance which appears across a reverse biased junction of a diode is called[ ]

a) diffusion b) transition c) drift d) none

12. The static resistance of a diode is the ratio of _____ to _____ [ ]

a) V to I b) I to V c) R to I d) None

13. The dynamic resistance of a diode is the ratio of _____ to _____ [ ]

a) I to V b) Change in voltage to change in current c) I to R d) none

14. In the steady state condition the current which flows through the diode is a _____ current.[ ]

a)diffusion b) static c) Both d) none

15. The _____ current results from the gradient of the minority carriers [ ]

a) static b) diffusion c) Both d) none

16. At large current amplitudes the diode behaves as combination of a _____ & _____[ ]

a) R,L b) C,R C) L,C d) none

17. At intermediate currents the diode behaves as a _____ & _____ [ ]

a) R b) C c) L d) all

18. Once break down occurs the diode current can be controlled only by the resistance of the [ ]

a) external circuit b) internal circuit c) Both d) none

19 BV_{CBO} is a characteristic of the _____ alone [ ]

a) transistor b) diode c) both d) none

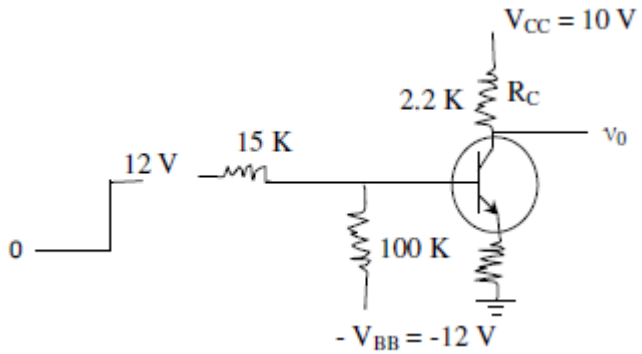
20. BV_{CEO} = _____ BV_{CBO} [ ]

a) $n\sqrt{}$ $1/h_{FE}$ b) $1/ h_{FE}$ c) h_{FE} d) none

11.4.3.3 TUTORIAL TOPICS

1 Design a transistor switch, with the following data. V_{CC} = 10 V; V_{BB} = 6 V; $I_{C\,sat}$ = 10 mA, $(hFE)_{min}$ = 30, Given NPN silicon transistor with negligible I_{CBO}. Assume junction voltages.

2 Show that the circuit given below works as a switch. Assume junction voltages and $(h_{FE})_{min}$ = 30.



5.4.4 UNIT-IV

5.4.4.1 DESCRIPTIVE QUESTIONS

1. In the nonsaturated binary shown in figure 4, the avalanche diodes D1 and D2 are nominally identical, as are diodes D3 and D4. The breakdown voltage V?Z of D3 and D4 is larger than the breakdown voltage Vz of D1 and D2. Verify that the transistors do not enter

the saturation region. Assume that D3 and D4 are always in the breakdown region and that either D1 or D2 but not both, is in the breakdown region. Then verify these assumptions.

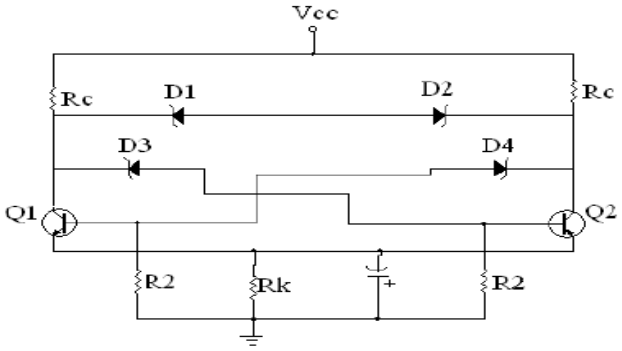


Figure 4

2. (a) Consider the symmetrical emitter triggering circuit of the figure 4 with Rc=3Re, R_1=2R2, and V_{CC}=6V. Indicate all the circuit voltages in the quiescent state and indicate also the voltages immediately after a 5-V positive step is applied. Assume that D3 and D4 are always in the breakdown region and that either D1 or D2 but not both in the breakdown region.

(b) Repeat part (a) for a 25-V step. What limits the maximum size of the input step? What limits the minimum size of the input step?

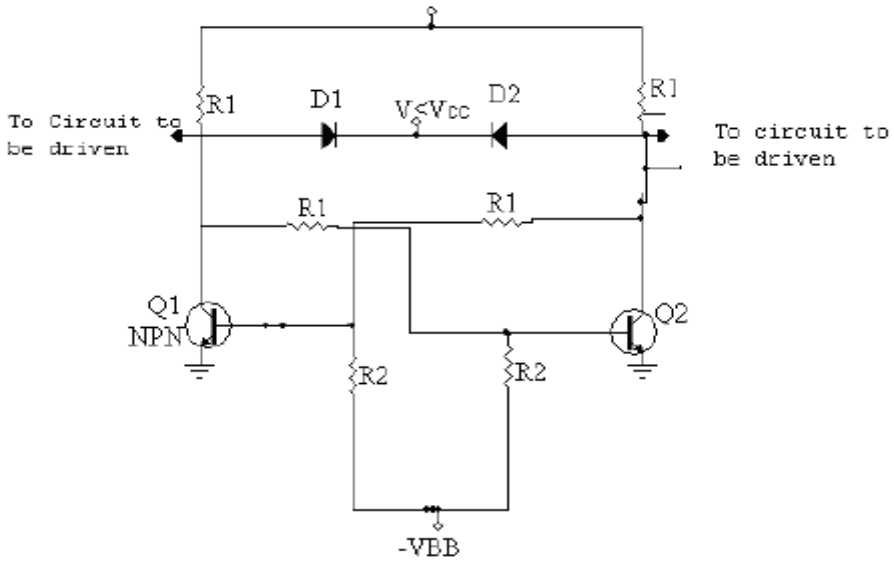


Figure 4

3. (a) Draw the circuit diagram of a Schmitt trigger circuit and explain its operation. Derive the Expressions for its UTP and LTP.

(b) Explain how an Schmitt trigger circuit acts as a comparator.4. In the monostable circuit of the given figure 4 the resistor R is connected to an auxiliary supply V_1 instead of V_{YY} . If A2 is in saturation or clamp and if A1 is OFF in the stable state, verify that the gate time T is given by Eq. $T = \tau \ln(V_{YY}+I_1R_Y-V\sigma)/(V_{YY}-V\gamma)$ with V_{YY} replaced by V_1.

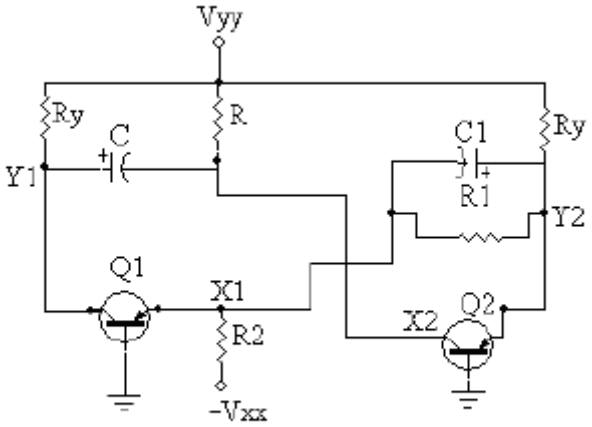


Figure 4

5. What is a monostable multivibrator? Explain with the help of a neat circuit diagram the principle of operation of a monostable multi, and derive an expression for pulse width. Draw the wave forms at collector and Bases of both transistors.

6. Draw and explain about the response of Schmitt circuit for the following.

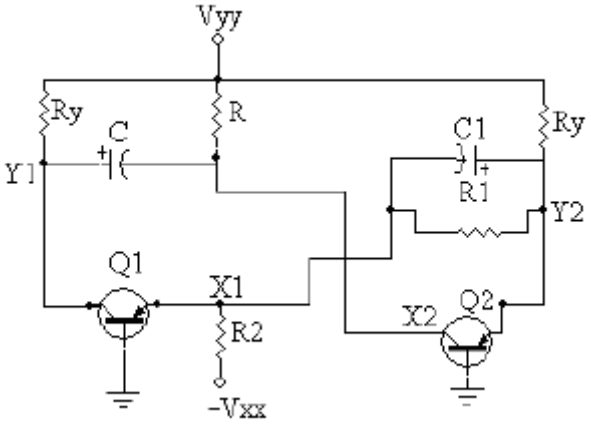
(a) for loop gain _1

(b) loop gain >1.

7. (a) Draw the circuit of a bistable multivibrator with symmetrical collector triggering.

(b) Design a monostable circuit that produces a pulse width of 10msec. (Assume the required date)

8. In the monostable circuit of the given figure 4 the resistor R is connected to an auxiliary supply V_1 instead of V_{YY} . If A2 is in saturation or clamp and if A1 is OFF in the stable state, verify that the gate time T is given by Eq. $T = \tau \ln(V_{YY}+I_1R_Y-V\sigma)/(V_{YY}-V\gamma)$ with V_{YY} replaced by V_1.



9. (a) The fixed-bias bistable multivibrator uses n-p-n transistors with h_{FE} = 20. The circuit parameters are

V_{CC} = 12 V, V_{BB} = 3 V, R_C = 1 K _, R_1 = 5 K _, R_2 = 10 K _. $V_{CE(sat)}$ = 0.4 V and $V_{BE(sat)}$ = 0.8 V. Find the stable

state voltages and currents.

(b) Draw the neat circuit diagram of a collector – coupled monostable multivibrator and explain its

operation with the help of waveforms.

10. (a) With the help of a neat circuit diagram and waveforms explain the working of collector-coupled astable multivibrator.

(b) Design a collector-coupled monostable multivibrator with a gate width of 3ms, using n-p-n transistors and V_{cc} = 6V, V_{BB}=3V, $I_{c\ sat}$ = 4 mA , $(h_{FE})_{min}$=40. Assume junction voltages.

11. (a) Draw the circuit diagram of Schmitt trigger and explain its working with the help of wave forms.

(b) Design a collector coupled bistastable mutlivibrator to meet the following specifications, $V_{CC} = V_{BB}$ =12V, I_C (sat) = 6mA, h_{FE} (min) = 30. Assume junction voltages.

12. A collector-coupled monostable multivibrator using n-p-n silicon transistors has the following parameters. V_{cc}= 12 V,V_{BB}= 4 V, R_c=1k_, $R_1=R_2=R$=15 k_. h_{FE}=35, r'_{BB}= 220_ and C=1000 PF. Neglect I_{CBO}. Calculate and plot to scale the wave shapes at each base and collector. Find the width of the output pulse.

ASSIGNMENT QUESTIONS

1 Draw the circuit of a Schmitt trigger circuit &explain its operation , Derive the expression forUTP&LTP

2 Draw the circuit of a Bistable Multivibrator circuit &explain its operation

9.4.4.2 OBJECTIVE QUESTIONS

1 A bistable multivibrator is also called [ ]

a)Eccles Jordan circuit b)binary c)trigger d)all

2. A Schmitt trigger is used as [ ]

a) Monostable multivibrator b) astable multivibrator c) none

3. In the stablestate the loopgain is [ ]

a)<1 b)=1 c)>1 d)=0

4. During transition the loopgain is [ ]

a)<1 b)=1 c)>1 d)=0

5. For hysterisis to exist in a Schmitt trigger, the loopgain must be [ ]

a)<1 b)>1 c)=1 d)=0

6. For ekimination of hysterisis in a Schmitt trigger, the loopgain must be [ ]

a)<1 b)=1 c)>1 d)=0

7. Which multivibrator can be used as a gating circuit [ ]

a) Bistable b) monostable c) Astable d) Schmitt trigger

8. Which multivibrator is called a free running circuit [ ]

a) Bistable b) monostable c) Astable d) Schmitt trigger

9. Which multivibrator can be used as a voltage to frequency convertor [ ]

a) Bistable b) monostable c) Astable d) Schmitt trigger

10. In bistable multivibrators the coupling elements are [ ]

a)Both capacitors b) Both resistors c)One capacitor & one resistor d)None

11. In mono stable multivibrators the coupling elements are [ ]

a)Both capacitors b) Both resistors c)One capacitor & one resistor d)None

12. In astable multivibrators the coupling elements are [ ]

a)Both capacitors b) Both resistors c)One capacitor & one resistor d)None

13. Which multivibrator is called a flip flop [ ]

a) Bistable b) monostable c) Astable d) none

14. Which multivibrator can be used as a memory element [ ]

a) Bistable b) monostable c) Astable d) Schmitt trigger

15. The astable multivibrator requires [ ]

a) Symmetrical triggering b)un Symmetrical triggering c)no triggering d)none

16. The resolution time is the sum of [ ]

a) Trasisition time b)Settling time c) both d) none

17. A Quasi stable state means a [ ]

a) Temperorly stable state b) permanent stable state c) no stable state d)none

18. The mono stable multibibrator is called a [ ]

a)one-shot b) single cycle c)uni vibrator d) none

19. The Astable multibibrator is used as [ ]

a) Master oscillator b) Schmitt trigger c) flip flop d) none

20. A Schmitt trigger is used as [ ]

a) Amplitude comparator b) binary c) both d) none

5.4.4.3 TUTORIAL TOPICS

1. Design a collector coupled bistastable mutlivibrator to meet the following specifications, $V_{CC} = V_{BB} = 12V$, I_C (sat) = 6mA, h_{FE} (min) = 30. Assume junction voltages.

2. A collector-coupled monostable multivibrator using n-p-n silicon transistors has the following parameters. V_{cc}= 12 V,V_{BB}= 4 V, R_c=1k_, R_1=R_2=R=15 k_. h_{FE}=35, r'$_{BB}$= 220_ and C=1000 PF. Neglect I_{CBO}. Calculate and plot to scale the wave shapes at each base and collector. Find the width of the output pulse.

9.4.5 UNIT-V

9.4.5.1 DESCRIPTIVE QUESTIONS

1. (a) Draw and clearly indicate the restoration time and flyback time on the typical waveform of a time base voltage.

(b) Derive the relation between the slope, transmission and displacement errors

(c) Explain how UJT is used for sweep circuit?

2. (a) Explain the basic principles of Miller and bootstrap time base generators.

(b) A transistor bootstrap ramp generator is to produce a 15V, 5ms output to a 2kohms load resistor. The ramp is to be linear within 2%. Design a suitable circuit using V_{cc} = 22V, $-V_{EE}$ = -22V and transistor with $h_{fe(min)}$ = 25. The input pulse has an amplitude of -5V, pulse width = 5ms and space width = 2.5ms.

3. (a) How are linearly varying current waveforms generated?

(b) In the boot strap circuit shown in figure5 V_{cc} = 25 V, V_{EE} = -15 V, R = 10 K ohms, R_B = 150 K ohms, C = 0.05 μF. The gating waveform has a duration of 300 μs. The transistor parameters are h_{ie} = .1Kohms, h_{re} = 2.5 x 10^{-4} K ohmsh_{fe} =50 h_{oe} = 1/40K ohms.

i. Draw the waveform of IC1 and Vo , labeling all current and voltage levels,

ii. What is the slope error of the sweep?

iii. What is the sweep speed and the maximum value of the sweep voltage?

iv. What is the retrace time Tr for C to discharge completely?

v. Calculate the recovery time T1 for C1 to recharge completely.

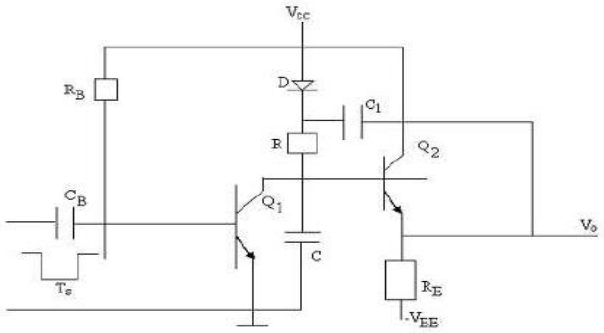


Figure 5

4. (a) With the help of a neat circuit diagram and waveforms explain the working of a transistor Miller time base generator.

(b) Find the component values of a bootstrap sweep generator, given Vcc=18V, Ic(sat) = 2mA and hfe(min)=30.

5. (a) Compare the principle of operation of Miller sweep circuit and Bootstrap sweep circuit

(b) Explain how linearity is obtained by adjusting the driving waveform of current sweep circuit.

6. (a) Define sweep-speed error, the displacement error and the transmission error.

(b) Draw the circuit diagram of transistor bootstrap time base generator and explain its working with the help waveforms.

7. (a) Define the terms slope error, displacement error and transmission error. How are they related for an exponential sweep circuit? Define the relation between them.

(b) With the help of a neat circuit diagram, explain the working of a transistor current time-base generator.

8.(a) With the help of a neat circuit diagram, explain the working of a simple transistor current Time –base base generator.

(b). Draw the circuit diagram of transistor constant current sweep circuit and explain its working. Derive an expression for the sweep speed error.

ASSIGNMENT QUESTIONS

1. Draw the circuit of bootstrap timebae generator and explain its operation
2. Draw the circuit of miller timebae generator and explain its operation

5.4.5.2 OBJECTIVE QUESTIONS

1. The input impedance of bootstrap integrator is

(a) low (b) high (c) Too high (d) moderate

2. The error e_t is represented by

(a) $e_t = \frac{(V_s^1)}{V_s}$

(b) $e_t = (V_s^n - V_s^1)$

(c) $e_t = \frac{(V_s' - V_s'')}{V_s}$

(d) $e_t = \frac{(V_s' - V_s)}{V_s}$

3. The input impedance of bootstrap integrator is

(a) low (b) high (c) moderate (d) Too high

4. Sweep speed error is defined as

(a) initial ramp speed/final ramp speed (b) initial ramp speed-final ramp speed/ initial ramp speed

(c) initial ramp speed +final ramp speed/initial ramp speed (d) final ramp speed/ initial ramp speed

5. Waveform can have either positive slope or negative slope

(a) Ramp (b) square (c) Trapizoidal (d) Rectangular

6. The variations in phase delay occur due to variations in factors like and

(a) Q point only (b) current gain & voltage gain (c) Q-point, supply voltage and gain

(d) loop gain, suply voltage and transistor parameters

7. The sweep voltage waveform has a solid waveform whose natural Period is given by

(a) $T_0 > T$ (b) $1/T_O$ (c) T_0 (d) $T_0 < T$

8. The duration during which the voltage level decreases to the initial level is Known as

(a) Trace (b) Retrace interval (c) sweep interval (d) Signal reconstruction

9. Difference between the input and output divided by the input is called as

(a) transistor error (b) transmission error (c) translational error (d) translational & transmission error

10. Current time base generators are used in

(a) In Radar screen scanning (b)TV scanning (c) Sonar application (d) where large raster area is to be scanned

11. In integrator neither terminals of the capacitor are connedcted to ground

(a) Emitter follower (b) Source follower (c) Bootstrap (d) Miller Integrator

12. The biggest advantage of Triggered sweep circuit is

(a) slow wave operation (b) Free running operation (c) Comlex operation (d) Fast running operators

13. Slope error is given by
(a) final slope/initial slope (b) initial slope+final slope/final slope
(c) initial slope-final slope/initial slope (d) Initial slope/final slope
14. The biggest disadvantage of Bootstrap using Darlington circuit is
(a) gain greater than unity (b) gain of the composite amplifier is smaller than each stage
(c) gain less than unity (d) gain of comosite amplifier is too large
15. Millers sweep circuit produces type of waveform
(a) negative going ramp (b) Sinusodalwave (c) positive going ramp (d) squarewave
16. Millers Integrator generates a ramp voltage
(a) sinusoidal (b) non-linear (c) linear (d) Cosinusoidal
17. The error arising due to transmission through a linear network is known as .transmisssion error
(a) Transmission error (b) True (c) Sweep error (d) False
18. Current time base generators are used in
(a) In Radar screen scanning (b) TV scanning (c) Sonar application
(d) where large raster area is to be scanned
19. For a basic Bootstrap integrator the transistor is connected as
(a) common base (b) common emitter (c) Common collector configuration (d) emitter follower
20. In a miller Integrator the capacitor is present in
(a) inputside (b) feedback (c) across output (d) output is inseries with capacitor
21. Slope error is given by
(a) final slope/initial slope (b) Initial slope/final slope
c) initial slope-final slope/initial slope (d) initial slope+final slope/final slope
22. Bootstrap sweep circuit employs feedback and miller Sweep circuit employs feed back.
(a) negative, negative (b) negative, positive (c) positive, negative (d) positive, positive

5.4.5.3 TUTORIAL TOPICS

1 A transistor bootstrap ramp generator is to produce a 15V, 5ms output to a 2kohms load resistor. The ramp is to be linear within 2%. Design a suitable circuit using V_{cc} = 22V, $-V_{EE}$ = -22V and transistor with $h_{fe(min)}$ = 25. The input pulse has an amplitude of -5V, pulse width = 5ms and space width = 2.5ms.

2. In the boot strap circuit shown in figure5 V_{cc} = 25 V, V_{EE} = -15 V, R = 10 K ohms, R_B = 150 K ohms, C = 0.05 μF. The gating waveform has a duration of 300 μs. The transistor parameters are h_{ie} = .1Kohms, h_{re} = 2.5 x 10^{-4} K ohmsh_{fe} =50 h_{oe} = 1/40K ohms

5.4.6 UNIT-VI

5.4.6.1 DESCRIPTIVE QUESTIONS

1. (a) What do you mean by synchronization ?
(b) What is the condition to be met for pulse synchronization?
(c) Compare sine wave synchronization with pulse synchronization?

2. (a) Explain the factors which influence the stability of a relaxation divider with the help of a neat waveforms.
(b) A UJT sweep operates with Vv = 3V, Vp=16V and η=0.5. A sinusoidal synchronizing voltage of 2V peak is applied between bases and the natural frequency of the sweep is 1kHz, over what range of sync signal Frequency will the sweep remain in 1:1 synchronism with the sync signal?

3. (a) What is relaxation oscillator? Name some negative resistance devices used as relaxation oscillators and give its applications.
   (b) With the help of a circuit diagram and waveforms, explain the frequency division by an astable multivibrator?
4. (a) Explain how monostable multivibrator is used as frequency divider?
   (b) Draw and explain the block diagram of frequency divider without phase jitter.

ASSIGNMENT QUESTIONS

1 What do you mean by a relaxation circuit ?Give a few examples of relaxation circuits
2 With the help of neat waveforms,explain sine wave frequency division with a sweep circuit

5.4.6.2 OBJECTIVE QUESTIONS

1. When two generators with equal frequencies run in synchronism the Synchronisation is said to be on a

(a) one-to many (b) multiplexing (c) one-to-one basis (d) many to one

2. When two generators produce waveforms at different frequencies, it is Essential for proper synchronisation that the frequency of one generator is an of that of the other generator.

(a) odd multiples (b) secondary harmonies (c) even multiples (d) intergral multiple

3. If synchronisation is achieved with different frequencies , ie., one Frequency being twice the other then it is termed as

(a) frequency matching (b) No synchronization occurs (c) synchronisation
(d) synchronisation with frequency division

4. The phenomenon of charging and discharging of a capacitor in a pulse digital circuit is called as

(a) Relaxation circuit (b) Timing circuit (c) Stable circuit (d) unstable circuit

5. If synchronisation is achieved with different frequencies , ie., one Frequency being twice the other then it is termed as

(a) No synchronization occurs (b) frequency matching s(c) synchronisation
(d) synchronisation with frequency division

6. When two generators with equal frequencies run in synchronism the Synchronisation is said to be on a

(a) many to one (b) one-to-one basis (c) one-to many (d) multiplexing

7. If synchronisation is achieved with different frequencies , ie., one Frequency being twice the other then it is termed as

(a) No synchronization occurs (b) synchronization (c) frequency matching
(d) synchronisation with frequency division

8. Synchronisation of sweep circuit can be obtained by

(a) Non identical phase signals (b) identical phase signals (c) Symmetrical signals
(d) unsymmetrical signals

9. Monostable relaxation circuit is used as a

(a) time division (b) both time and frequency (c) frequency division (d) only frequency multiplexing

10. By making ————————, a divider circuit with a division factor n can be built

(a) $T_O < nT_p$ (b) $T_O > nT_p$ (c) $T_O = 2nT_p$ (d) $T_O = nT_p$

11. When two generators with equal frequencies run in synchronism the Synchronisation is said to be on a

(a) many to one (b) multiplexing (c) one-to many (d) one-to-one basis

12. stray signals are

(a) Introducing distorition (b) affects synchronisation severely (c) does't affect sychronization

(d) unwanted noisy signals

13. In a Sinusoidal synchronisation signal UJT is used as a switch beause

(a) negative resistnce voltage controlled device (b) negative resistance current controlled device

(c) voltage divider (d) Current divider

14. generators can be triggered and synchronised

(a) Saw-tooth (b) square (c) Sinewave (d) Ramp

15. When two generators with equal frequencies run in synchronism the Synchronisation is said to be on a

(a) many to one (b) multiplexing (c) one-to-one basis (d) one-to many

16. The condition for proper transimission in a frequency division without phase Jitter is given by

(a) Tp < Tg < 2Tp (b) 2Tg<Tp (c) Tp > Tg > 2Tp (d) Tp > 2Tg

17. By making ————————, a divider circuit with a division factor n can be built

(a) $T_O = 2nT_p$ (b) $T_O < nT_p$ (c) $T_O > nT_p$ (d) $T_O = nT_p$

18. Phase jitter affects

(a) pulses of order millisecs (b) pulses of order of microsec (c) narrow pulses of the order of picosecs (d) pulses of order nano secs

19. stray signals are

(a) affects synchronisation severely (b) unwanted noisy signals (c) does't affect sychronization

(d) Introducing distorition

20. Between the instant of occurance of the pulse which prematurely terminates the cycle and the instant of the change of state of the oscillator there is certain time delay. This is termed as

(a) phase delay (b) sync delay (c) delay (d) lagging

5.4.6.3 TUTORIAL TOPICS

1 A UJT sweep operates with Vv = 3V, Vp=16V and η=0.5. A sinusoidal synchronizing voltage of 2V peak is applied between bases and the natural frequency of the sweep is 1kHz, over what range of sync signal frequency will the sweep remain in 1:1 synchronism with the sync signal?

9.4.7 UNIT-VII

9.4.7.1 DESCRIPTIVE QUESTIONS

1. (a) Why are sampling gates called Selection circuits?
   (b) What are the advantages of unidirectional sampling gates?
   (c) What are the applications of sampling gates?

2. (a) What is sampling gate? Explain how it differ from Logic gates?
   (b) What is pedestal? How it effects the output of a sampling gates?
   (c) What are the drawbacks of two diode sampling gate?

3. (a) Why are sampling gates called linear gates?
   (b) What are the other names of a gate signal?
   (c) Compare the unidirectional and bi-directional sampling gates.

4. (a) Explain the balance conditions in a bi-directional diode gate.
   (b) Explain the utility of sampling gate in a sampling scope.

ASSIGNMENT QUESTIONS

1 (a) What is a sampling gate? Explain how it differs from Logic gates?
(b) What is pedestal? How it effect the output of sampling gates

5.4.7.2 OBJECTIVE QUESTIONS

1. The variations in phase delay are called as
   (a) Sampling gates (b) phase jitters (c) phase shifters (d) Blocking jitters
2. Sampling gate for which input voltage is
   (a) ac only (b) Sampling of acsignal (c) dc only (d) Either dc or ac
3. Advantages of Diode sampling gate over the transister Sampling gate are
   (a) Linearity only (b) Non-linearity of operation and elimination of pedestal
   (c) Linearity of operation and elimination of pedestal (d) stable operating point achievement
4. Chopper amplifier is also known as
   (a) modulator (b) signal generator (c) Non-linearwave form generator (d) Waveform generator
5. The interval of time is selected by means of an externally aplied signal is Termed as
   (a) ramp (b) square wave (c) sync pulse (d) gating signal
6. The biggest disadvantage of sampling gate is
   (a) the slow rise of control voltage (b) the slow rise of control current (c) Risetime fall time
   (d) fast rise of control voltage

7. The gain of bidirectional gate is given by

   (a) $A = \{ 2R_L\alpha \} / [R_L - R_3/2]$
   (b) $\{ a /(R_L + 2R_3 \}$
   (c) $[\alpha R_L] / [R_L - R_3/2]$
   (d) $\left\{ \left[\frac{R_L}{R_L + R_3/2} \right] \alpha \right\}$

8. A sampling gate is also termed as
   (a) linear gate (b) time-selection gate (c) time selection & linear gates (d) non-linear gate
9. The controlling digital signal is also referred to as
   (a) gating signal (b) ligic signal (c) Trigger signal (d) control signal

10. Sampling gate for which input voltage is

(a) dc only (b) Sampling of acsignal (c) ac only (d) Either dc or ac

11. The time interval for transmission is selected by means of an externally applied signal Called as

(a) Gating signal (b) control signal (c) Logic signal (d) Threshold signal

12. The gain of bidirectional gate is given by

(a)nhR_L R_L+ R_3 /2i_o (b) { a /(R_L + 2R_3 } (c) A = { 2R_L_} / [R_L - R_3 /2] (d) [_R_L] / [R_L - R_3/2]

13. A Sampling gate which can handled the input signal excursion of both polarities is termed as

(a) multidirectional gate (b) n-directional gate (c) Bi-directional gate (d) unidirectional gate

14. The parametres of a Non-ideal switch are

(a) Analog channel & digital control line control parameters (b) Analog & Digital

(c) Digital and analog control (d) Digital switch control

15. Chopper amplifier is also known as

(a) Waveform generator (b) modulator (c) signal generator (d) Non-linearwave form generator

16. The biggest disadvantage of sampling gate is

(a) the slow rise of control voltage (b) the slow rise of control current (c) fast rise of control voltage

(d) Risetime fall time

17. The time interval for transmission is selected by means of an externally applied signal Called as

(a) Gating signal (b) control signal (c) Logic signal (d) Threshold signal

18. Q15 In fourdiode Sampling gate V_{nmin} is given by

(a) $\left[\frac{V\,R2}{RC+R2}\right]$

(b) $\left[\frac{V_s\,RC}{Re+R2}+\frac{V\,R2}{Re+R2}\right]$

(c) $\left[\frac{V_s RC}{RC+R2}\right]$

(d) $\left[\frac{V_s\,RC}{Re+R2}-\frac{V\,R2}{Re+R2}\right]$

19. Sampling gate is also known as

(a) Non-linear gate (b) Transmission gate (c) frequency selection gate (d) log gate

20. Modes of operation of Blocking oscillators are

(a) Bistable mode (b) stable mode (c) astable mode (d) Triggered mode

21. Sampling gate can not be used as a

(a) Multiplexer (b) Sampling Scope (c) D to A converter (d) A to D converter

22. The interval of time is selected by means of an externally aplied signal is Termed as

(a) gating signal (b) ramp (c) sync pulse (d) square wave

5.4.7.3 TUTORIAL TOPICS

1 Draw the circuit diagram of bidirectional diode sampling gate and explain its working. Derive expressions

for gain A, control voltage V_C and control voltage Vn.

UNIT-VIII

5.4.8.1 DESCRIPTIVE QUESTIONS

1. (a) With the help of circuit diagram explain the purpose of clamping diode in a positive diode AND gate.

(b) Explain the effect of and diode capacitance on the output pulse of diode AND gate.

2. (a) Draw and explain the circuit diagram of integrated positive RTL NOR gate

(b) Compare the RTL and DTL logic families in terms of Fan out, propagation delay, power dissipated per gate and noise immunity.

3. (a) Why totem pole is used in DTL? Draw the circuit diagram and explain a DTL gate with this.

(b) Verify the truth table of RTL NOR gate with the circuit diagram of two inputs.

4 (a) What are the basic logic gates which perform almost all the operations in Digital communication systems.

(b) Give some applications of logic gates. (c) Define a positive and negative logic systems.

(d) Draw a pulse train representing a 11010111 in a synchronous positive logic digital system.

ASSIGNMENT QUESTIONS

2 (a) What are the basic logic gates which perform almost all the operations in Digital communication systems (b) Give some applications of logic gates (c) Define a positive and negative logic system

5.4.8.2 OBJECTIVE QUESTIONS

1. Complementary output is available in which of the following logic families

(a) TTL (b) DTL (c) ECL (d) RTL

2. Which of the following flip-flops is used as latch

(a) ECL (b) TTL (c) ISL (d) CMOS

3. An AND gate is a

(a) Multiplexing circuit (b) sequential circuit (c) combinational circuit (d) Memory circuit

4. Two similar RTL gates are wire-ANDed. What will be the fan-out of the Combined gate if each has fan-out of 5?

(a) five (b) two (c) eight (d) ten

5. The cost of Schottky clamped TTL is ————-

(a) low (b) average (c) very high (d) moderate

6. An IC that is a 4-bit latch is

(a) 7400 (b) 7446 (c) 7410 (d) 7475

7. The value of Boolean expression X.X.X.X . $\bar{X}$ is ————

(a) Zero (b) – 1 c) 1 (d) X

8. The Figure relates to which logic implementation?

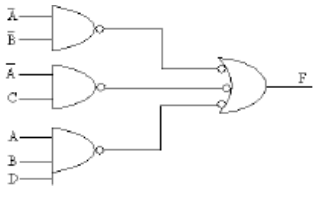


Figure 20

(a) OR (b) XOR (c) NAND (d) NOR

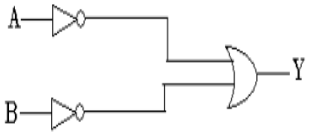
9. ———— operating speed is usually the main requirement of digital IC's

(a) Very low (b) Moderate (c) Very high (d) High

10. The ECL can be used to switch frequencies as high as

(a) 500MHz (b) 1GHz (c) 1MHz (d) 100MHz

11. The output of the circuit given figure below is

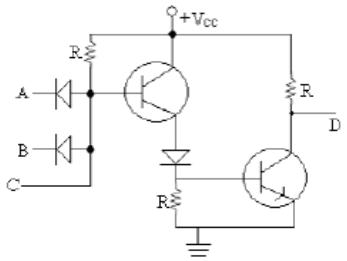


(a) 10 (b) 00 (c) 01 (d) 11

12. Differential signals are used in the following logic family

(a) .RTL (b) DTL (c) TTL (d) ECL

13. The Figure refers to logic

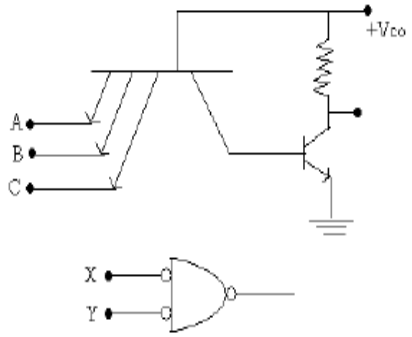


(a) RTL (b) ECL (c) DTL (d) TTL

14. Complementary output is available in which of the following logic families

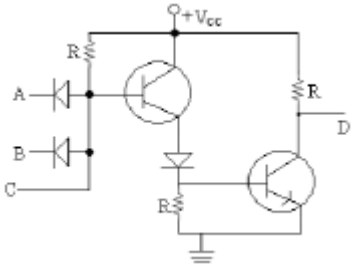
(a) RTL (b) TTL (c) ECL (d) DTL

15. The logic operations of the two circuits givenFigure below are



(a) identical (b) entirely different (c) Non- Identical inverter (d) complementary

16. The Figure refers to logic



(a) DTL (b) ECL (c) TTL (d) RTL

17. The ECL can be used to switch frequencies as high as
(a) 100MHz (b) 1MHz (c) 1GHz (d) 500MHz

18. Which of the following logic has the fan-out more than 90
(a) TTL (b) 8ns ECL (c) 4nsECL (d) CMOS

19. Which of the following is the oldest and slowest type ?
(a) NMOS (b) PMOS (c) CMOS (d) Bi-CMOS

20. The IC 7446 whose function is
(a) multiplexer (b) OR gate (c) encoder (d) BCD-to- Seven Segment display

21. The IC 7402 refers to ——————
(a) XNOR (b) XOR (c) NOR (d) NAND

22. A is basically a transmision circuit which allows input signal to pass through it during selected

interval and blocks its passage outside this this time interval.

(a) XOR gate (b) Sampling gate (c) OR gate (d) nor gate

23. Power dissipation of logic family is defined as the supply power required for the gate to operate
with ——————duty cycle at a certain specified frequency
(a) 50% (b) 25% (c) 100% (d) 75%

24. Fan-in for a TTL gate is given by
(a) 5 (b) 8 (c) 6 (d) 7

25. A NAND circuit with positive logic will operate as
(a) NOR with negative logic (b) AND with negative logic (c) AND with positive logic
(d) OR with negative logic

26.A is basically a transmision circuit which allows input signal to pass through it during selected
interval and blocks its passage outside this this time interval.
(a) Sampling gate (b) OR gate (c) XOR gate (d) nor gate

27. Typical Noise margin for DTL family is
(a) 0.7 (b) 0.72 (c) 0.2 (d) 0.07

28. The biggest advantage of TTL gate is
(a) Fast and Complicate to use (b) Fast and easy to use (c) slow and simple to use
(d) wide selection of circuit available

29. The IC 7446 whose function is
(a) BCD-to- Seven Segment display (b) multiplexer (c) encoder (d) OR gate

30. The feature Active-pull-Up and Active Pull-Down is available in ———-
(a) RTL (b) DTL (c) ECL (d) TTL

5.4.8.3 TUTORIAL TOPICS

1 a) What are the basic logic gates which perform almost all the operations in Digital communication systems.

(b) Give some applications of logic gates. (c) Define a positive and negative logic systems.

(d) Draw a pulse train representing a 11010111 in a synchronous positive logic digital system

6. SWITCHING THEORY AND LOGIC DESIGN

6.1 JNTUH SYLLABUS

UNIT I NUMBER SYSTEMS AND CODES: Philosophy of number systems complement representation of negative numbers binary arithmetic binary codes error detecting and error correcting codes hamming code.

UNIT II BOOLEAN ALGEBRA AND SWITCHING FUNCTIONS: Fundamental postulates of Boolean Algebra Basic theorems and properties switching functions Canonical and Standard forms Algebraic simplification digital logic gates, properties of XOR gate universal Gates Multilevel NAND/NOR realizations.

UNIT III MINIMIZATION OF SWITCHING FUNCTIONS: Map method, Prime implicants, Don't care combinations, Minimal SOP and POS forms, Tabular Method, Prime Implicant Chart, simplification rules.

UNIT IV COMBINATIONAL LOGIC DESIGN: Design using conventional logic gates, Encoder, Decoder, Multiplexer, De Multiplexer, Modular design using IC chips, MUX Realization of switching functions partly bit generator, code converters, Hazards and hazard free realizations.

UNIT V PROGRAMMABLE LOGIC DEVICES, THRESHOLD LOGIC: Basic PLD'SROM, PROM, PLA PLD Realization of Switching functions using PLD'S. Capabilities and limitations of Threshold gate. Synthesis of Threshold functions, Multigate Synthesis.

UNIT VI SEQUENTIAL CIRCUITS I: Classification of sequential circuits (Synchronous, Asynchronous, Pulse mode, Level mode with examples) Basic flip flops Triggering and excitation tables. Steps in synchronous sequential circuit design. Design of modulo Ring and Shift counters, Serial binary adder, sequence defector.

UNIT VII SEQUENTIAL CIRCUITS II: Finite state machine capabilities and limitations, Mealy and Moore models – minimization of completely specified and incompletely specified sequential machines, Partition techniques and Merger chart methods concept of minimal cover table.

UNIT VIII ALGOROTHIMIC STATE MACHINES: Salient features of the ASM char –Simple example System design using data path and control implementations examples of Weighing machine and Binary multiplier.

TEXTBOOKS:

1. Switching and Login design CVS Rao, Pearson, 2005.
2. Switching and Finite Automata theory Zvi Kohavi, TMH, 2 nd Edition.

REFERENCES:

1. Introduction to Switching Theory and Logic Desogm F. J.Hill, G.R. Peterson, John Wiley, 2 nd Edition
2. Switching Theory and Logic Design R.P.Jain, TMH Edition, 2003.
3. Digital Design Morris Mano, PHI, 2 ND Edition.
4. An Engineering Approach To Digital Design Fletcher, PHI, Digital Logic Application and Design John M.Yarbrough, Thomson.

5. Fundamentals of Logic Design Charles H.Roth, Thomson Publlications, 5 th Edition, 2004.

6.2 UNIT WISE PLANNER FOR ACADEMIC YEAR 2013 - 2014

Subject: **Switching Theory And Logic Design**

Unit No.	**Date Planned to complete**	**Date Conducted**	**Remarks**
I			
II			
III			
IV			
V			
VI			
VII			
VIII			

6.3 SESSION PLANNER

Unit No.	S.No	Topic	Date Planned	Date Conducted	Remarks
I	**1**	Introduction			
	2	Philosophy of number systems Binary &decimal number system			
	3	Octal and hexadecimal number system			
	4	Binary addition and subtraction			
	5	Binary multiplication and division			
	6	1's complement representation of negative number			
	7	2's complement representation of negative number			
	8	binary codes			
	9	BCD addition			
	10	error detecting and error correcting codes			
	11	Hamming codes			
	12	Class test			
II	**1**	Fundamental postulates of Boolean Algebra			
	2	Basic theorems and properties			
	3	switching functions Canonical and Standard forms SOP			
	4	switching functions Canonical and Standard forms POS			
	5	Algebraic simplification digital logic gates & properties of XOR gate			

	6	universal Gates Multilevel NAND & NOR realizations			
	7	Class test			
III	**1**	Introduction to K-map			
	2	2,3&4 variable mapping			
	3	5 variable mapping & Don't care combinations			
	4				
	5	Minimal SOP and POS forms			
	6	Tabular Method			
	7	Prime Implicant Chart, simplification rules			
	8	Class test			
IV	**1**	Design using conventional logic gates			
	2	Encoder			
	3	Decoder			
	4	Multiplexer& Demultiplexer			
	5	Modular design using IC chips, MUX Realization of switching functions			
	6	party bit generator			
		code converters			
		Hazards and hazard free realizations			
		Class test			
V		Basic PLD'S ROM, PROM			
		PLA' S			
		PAL'S			

		Capabilities and limitations of Threshold gate			
		Synthesis of Threshold functions			
		Multigate Synthesis			
		Class test			
VI		Classification of sequential circuits			
		Basic flip flops			
		Triggering and excitation tables &Master slave J-K flip flop			
		Steps in synchronous sequential circuit design			
		Design of modulo counters			
		Ring &Johnson counter			
		Serial binary adder			
		sequence defector			
		Class test			
VII		Finite state machine capabilities and limitations			
		Mealy models			
		Moore models			
		minimization of completely specified and incompletely specified sequential machines: Partition techniques			
		Merger chart methods			
		concept of minimal cover table			
		Class test			
VIII		Salient features of the ASM chart – Simple example and			
		System design using data path			

		implementations			
		System design using control implementations			
		examples of Weighing machine			
		Binary multiplier			
		Class test			

6.4. QUESTION BANK

6.4.1UNIT-I

6.4.1.1 DESCRIPTIVE QUESTIONS

1. (a) Convert the following numbers:
   i. $(6753)_8$ to base 10
   ii. $(00111101.0101)_2$ to base 8 and base 4
   iii. $(95.75)_{10}$ to base 2.
   (b) Represent +65 and -65 in sign-magnitude, sign-1's complement and sign-2's Complement representation.
2. Given a = 10101001 and b = 1101 find:
   i. a + b
   ii. a - b
   iii. a . b
   iv. a / b.
3. What is the Gray code? What are the rules to construct Gray code? Develop the 4 bit Gray code for the decimal 0 to 15.
4. What are the rules for XS3 addition? Add the two decimal numbers 123 and 658 in XS3 code.

ASSIGNMENT QUESTIONS

1. Express the decimal digits 0-9 in BCD,2421,84-2-1 and Excess-3.
2. Convert the following number to be indicated bases

   a. 7562.45 to octal b.1938.257 to hexadecimal c. Add in BCD form 98 and 87

6.4.1.2 OBJECTIVE QUESTIONS

1. Number system used in digital equipment
   a.) Decimal b.)Binary c.) Hexadecimal d.) Octal
2. Gray code belongs to the class
   a.) Cyclic codes b.) Reflected codes c.) Both d.) None
3. Conversion of fractional number to any system is accomplished by

a.) Successive multiplication b.) Successive division c.) Both d.) None

4. Which of the following are Self Complementary 1) (6,4,2,-3) 2) (2,4,2,1) 3) (8,4,2,1) 4) (3,3,2,1)
   a.) 1&2 b.) 3 c.) 1,2&4 d.) 1&3
5. Excess-3 of BCD is obtained by adding _____ to BCD code
   a.) 1100 b.) 0011 c.) 1001 d.) 0110
6. For a code to be error detecting, the minimum distance between two successive code words is a.) zero b.) five c.) two d.) infinity
7. For a code to be error detecting, the minimum distance must be
   a.) one b.) two c.) three d.) four
8. The number of k parity digits need to satisfy the inequality
   a.) $2^k \geq m+k-1$ b.) $2^k \geq m+k$ c.) $2^k \geq m+k+1$ d.) $2^k \geq m-k$
9. 23+44+14+32=223. What would be the base of the above system
   a.) b=3 b.) b=4 c.) b=5 d.) b=5
10. 8421 and Excess-3 are
    a.) Weighted b.) Reflective c.) Alphanumeric d.) sequential
11. Binary equivalent of gray number 1110 is
    a.) 1011 b.) 1010 c.) 1100 d.) 0101
12. 1010P; for odd parity p=?
    a.) 0 b.) 1 c.) both d.) none
13. Even parity hamming code for 1101
    a.) 1100110 b.) 1001100 c.) 1010110 d.) 1010101
14. $FACE_{16}$ to binary
    a.) 1111011101001 b.) 1111101011001110 c.) 11111111100001 d.) 0111100000000110
15. $(0.4375)_{10}$ to binary
    a.) 0.0011 b.) 0.10010 c. 0.0111 d.) 11.0011
16. $(10011.11)_2 = X_{16}$; X=?
    a.) A.C b.) 13.A c.) C.12 d.) 13. C
17. Hamming code for decimal digit 1_{10}
    a.) 110011 b.) 001110 c.) 11011001 d.) 1101001
18. $(1431)_8 = (?)_{10}$
    a.) 793 b.) 344 c.) 391 d.) 395
19. $11001101.0101 = (?)_8$
    a.) 315.22 b.) 315.24 c.) 410.22 d.) 344.26

20. 1234+5432=6666. possible base is
    a.) 2b.) 3 c.) 4 d.) 5

6.4.1.3 TUTORIAL TOPICS

1. Discuss about number system the number system and their conversions.
2. Devise a single error correcting code for a 11 bit group 01101110101
3. Test the following Hamming code sequence for 11 bit message and correct it if necessary (1010010111 01011).

6.4.2 UNIT-II

6.4.2.1 DESCRIPTIVE QUESTIONS

1. State and prove the following Boolean laws:
   i. Commutative
   ii. Associative
   iii. Distributive.
2. Simplify the following Boolean functions to minimum number of literals:
   i. (a + b)' (a' + b')'
   ii. y(wz' + wz) + xy
3. State Duality theorem. List Boolean laws and their Duals.
4. Prove that OR-AND network is equivalent to NOR-NOR network and AND-OR network is equivalent to NAND-NAND network.

ASSIGNMENT QUESTIONS

1. For the given Boolean function F=xy'z+x'y'z+w'xy+wx'y+wxy

i. Draw the logic diagram ii. Simplify the function to minimal literals using Boolean algebra.

2. Draw the NAND logic diagram that implements the complement of the following function

F(A,B,C,D)= Σ(0,1,2,3,4,8,9,12).

6.4.2.2 OBJECTIVE QUESTIONS

1. $(a^1)^1$=

   a. a b.a^1 c.0 d.1

2. (x+y+z) =

   a. x+xyz b. (x+y)(x+z) c. xy+z d.xyz

3. $(x.y)^1$ =

   a.x^1+y b.x+y^1 c.x^1+y^1 d.x^1.y^1

4. $(x+y)^1$ =

a.x^1+y^1 b.$x^1.y^1$ c.$(x.y)^1$ d.x^1+y

5. If T_1 and T_2 are any two switching expressions which of the following is an invalid

Expression = _____.

a.$T_1.T_2$ b.T_1/T_2 c.$T_1{}^1+T_2$ d.$(T_1.T_2)$

6. Consensus theorem is = _____

a).$x+x^1=x+y$ b).$xy+x^1z+yz = xy+x^1z$ c).$xy+x^1z+yz = xy+yz$ d).$xy +yz +zx = x^1y+z^1x$

7.EX-OR algebraically can be stated as = _____

a.A^1B+AB^1 b.A^1B^1+AB c.$A^1B+A^1B^1$ d.none

8.$a+a^1b+a^1b^1c+a^1b^1c^1d+$..... in simplified form

a).$a^1+b^1+c^1+d^1+$... b).a^1+b+c^1+d+...c).$a+b+c+d+$..... d).$a+b^1+c+d^1+$....

9.$(a^1)^1$ is called _____

a. convolution b. complement over complement c.involution d.cosensus

10.Boolean algebra was developed by _____

a.John-bool b.George boole c. Ramanujan d.none

11.according to the consensus theorem $(x+y)(x^{1+}z)(y+z)$

a.$(x+y)(x+z)$ b.$(x+y)(x^1+z)$ c.$(x+z^1)(x+y)$ d.none

12.If $f(x,y,z) = \Sigma(0,2,3,5,7)$ then canonical product of sums will be

a. $f(x,y,z)=\Pi(0,1,4,6)$ b. $f(x,y,z)=\Pi(1,4,6)$ c. $f(x,y,z)=\Pi(0,1,4,5,6)$s d. $f(x,y,z)=\Pi(0,2,3,5,6)$

13. Two switching functions are said to be equivalent if and only if there canonical SOP are ____

a.equal b. not equal c.can't say d.none

14. What is the dual of consensus theorem

a. $A+B(A+B)(A+C)(B+C)=(AB)(A+C)$ b). $A+B(A+B)(A^1+C)(B+C)=(AB)(A+C)$

c. $A+B(A+B)(A^1+C)(B+C)=(AB)(A+C^1)$ d). none

15. The sum of 2^n minterms of n variable function is _____

    a. 0 b. 2n c. N d. 1

16. The product of any two different n variable minterm is

    a. 0 b. 2n c. N d. 1

17. The sum of any two different n variable maxterm is

    a. 0 b. 2n c. N d. 1

18. The dual of m3 is

    a. m3 b. M3 c. 0 d. 1

19. 1+A+AB+ABC+-------=

    a. 0 b. N c. A d. 1

20. $(A^1.B^1.C)^1$=

    a.ABC b.A^1+B^1+C c.$A+B+C^1$ d. A+B+C

6.4.2.3 TUTORIAL TOPICS

1. Discuss about the Boolean algebra.

2. Give three possible ways to express the function F = $A\ ^1B^1D^1$+ $A^1B^1C^1D^1$ + A^1BD + ABC^1D with eight or less literals.

6.4.3 UNIT-III

6.4.3.1 DESCRIPTIVE QUESTIONS

1. Simplify the following Boolean expressions using K-map and implement them using NOR gates:

   F (A, B, C, D) = AB'C' + AC + A'CD'

2. List the Boolean function simplification rules using Tabulation method.

3. Simplify the Boolean function using K-map and implement using NAND gates

   $F=\Sigma m(0,2,3,4,5,6)$

4. Reduce the given function using tabular minimization method

   $F(A,B,C,D)=\Pi(0,1,3,4,5,6,7,8,9)+d(10,11,12,13,14,15)$.

ASSIGNMENT QUESTIONS

1. Simplify the Boolean expression using K-map $F=A^1+AB+ABD^1+AB^1D^1+C$

2. Give the minimum two level SOP realization of the following switching function using only NAND gates $F(x,y,z)=\Sigma m(0,3,4,5,7)$.

6.4.3.2 OBJECTIVE QUESTIONS

1. The main theorem that is being applied in the K-map simplification is

   a)Demorgan's theorem b) Consensus theorem c) Combining theorem, $Aa+Aa^1=A$ d) None

2. In K-map,_____ code is used for fixing the value of a minterm

   a. Excess-3 b. 2421 c. 642-3 d. Cyclic

3. In the minimization using K-maps, sometimes one cell will be covered by more than one subcube, this can be justified by _____ law

   a. Associate law b. Distributive law c. Commutative d. Idempotent

4. The number of calls in a 4 variable K-map is

   a. 4 b. 16 c. 8 d. 3

5. For each cell, number of adjacent cells in a 4 variable K-map is

   a. 2 b. 4 c. 3 d. 8

6. Which of the following code is used in K-map for representing the minterms

   a. 8421 b. BCD c. Excess-3 d. Gray code

7. The minterm corresponding to decimal number 13 is

   a. ABCD b. $A+B+C^1+D$ c. $A^1+B+C+D$ d. $AB\,C^1D$

8. Six variable function contain_____ number of cells in a K-map

   a. 64 b. 32 c. 16 d. 8

9. What is the decimal position of the minterm $A^1B^1C^1D^1$ in the K-map

   a. 2 b. 0 c. 15 d. 14

10. If f(A,B,C,D)=1 then the K-map contains ____ _____ number of logic 1's is

    a. 4 b. 8 c.16 d. 32

11. In Tabular method, two terms from adjacent groups are combinable if their binary representation differs by a _____ digit in the same position

    a. Single b. Two c. Four d. None

12. In a tabular method the minimal expression of a function contains _____

    a) Only prime implicants b)Prime implicants and essential prime implicants

    c)Only essential prime implicants d)All variables

13. In a 4 variable K-map, the function contains all minterms, then the minimal expression is _

    a. A b. 1 c. 0 d. Don't care

14. Looping a pair of adjacent 1's in a K-map eliminates _____ number of variables

    a. 1 b. 2 c. N d.n-1

15. In a n-variable K-map, after looping a quad of adjacent 1's, the resultant term contains_____

    a. 1 b. 2 c. N-1 d. N-2

16. The complement of "minterm 4" is

    a. Maxterm 4 b. Minterm 0 c. Minterm 13 d. Maxterm 13

17. The resultant of the function cannot be further simplified is

    a. Minimal b. Irredundant c. either a or c d. None

18. The given maxterm is A+B+C, its equivalent binary represented is

    a. 101 b. 010 c. 111 d. 000

19. The given maxterm is A+B+C, its equivalent binary represented is

    a. 101 b. 010 c. 111 d. 000

20. A function F(A,B,C) contains minterms 1,2,3,5,6,7, its complement contains

    a. Σm (0,4)b. Σm(1,2,3,5,6,7) c. ΠM (1,2,3,5,6,7) d. ΠM (0,4)

6.4.3.3 TUTORIAL TOPICS

1. Simplify the function using Karnaugh map method
   F (A,B,C,D) =Σ(4,5,7,12,14,15)+Σd(3,8,10).
2. Reduce the following function using K- map and implement it in AOI logic as well as NOR logic F= ΠM(0, 1, 2, 3, 4, 7)

6.4.4 UNIT-IV

6.4.4.1 DESCRIPTIVE QUESTIONS

1. Implement the following Boolean functions using decoder and OR gates:

   F1(A,B,C,D) = _(2,4,7,9)
   F2(A,B,C,D) = _(10,13,14,15)
2. What is Hazard in switching circuits? Explain the design of Hazard free Switching circuit with an example
3. What is Encoder? Design Octal to Binary Encoder.

4. Design a combinational circuit that converts a decimal digit from 8, 4,-2,-1 code to 8,4,2,1 BCD code

ASSIGNMENT QUESTIONS

1. Design a Excess-3 adder using 4 bit parallel binary adder and logic gates.
2. Design a combinational circuit that accepts a 3 bit number and generates an output binary number equal to the square of the input number.

6.4.4.2 OBJECTIVE QUESTIONS

1. If an input A is given to the inverter, the output will be

   a. A b. A^1 c. 1 d. 0

2. Which gate is suitable for bit comparison

   a. Ex-OR b. AND c. EX-NOR d. OR

3. The difference bit output of a half subtractor is same as

   a. Difference bit of a full subtractor b.Sum bit of a half adder

   b. Sum bit of a full adder d.Carry bit of a half adder

4. A full adder can be realized as

   a. One half adder, two OR gates b.Two half adders, one OR gate

   b. Two half adders, two OR gate c.One half adder, one OR gates

5. The sum of expression in a half adder is

   a. X^1Y+XY^1 b. $(X+Y)(X^1+Y^1)$ c. $(C+X^1Y^1)^1$ d. All

6. In a carry look ahead adder, the carry at each stage (except in the initial stage) is a function of

   a. Carry propagate b. Carry generate c. Both d. None

7. BCD adder requires _____ no. Of full adders

   a. 1 b.2 c. 3 d. 4

8. _____ no of NAND gates are required to realize a half subtractor

   a. 5 b. 6 c. 7 d. 8

9. A decoder with n inputs produces maximum of _____- no of minterms

   a. 2^n b.2^n-1 c.2^{n-1} d. 2n

10. The general representation of encoder is _____(where m!=n and 2^n>m)

    a. 2^n:m b.m:2^n c.n:2^n d. 2^n:n

11. MUX is _____ implementation

    a. AND-OR b. OR-AND c. NAND-OR d. NOR-AND

12. MUX is represented by

    a. 2^n*1 b. 2^n*n c.$n*2^n$ d. $1*2^n$

13. DE-MUX is represented by

    a. 2^n*1 b. 2^n*n c.$n*2^n$ d. $1*2^n$

14. An XOR gate with 6 terms contains _____ no of minterms

    a. 6 b. 12 c. 64 d. 32

15. The minimum number of NAND gates required to implement the function $F=(x^1+y^1)(z+w)$

    a. 3 b. 4 c. 5 d. 6

16. If binary multiplication is to be implemented by using a two input gate, then it should be _____ gate

    a. EX-OR b. NOR c. AND D.OR

17. EX-OR followed by an inverter has the property

    a. Output high for input word of even parity b.Output high for input word of odd parity

    c. Output is 1's complement of input word d.Output is 2's complement of input word

18. Can more than one decoder output be activated at one time

    a. Yes b. no c. data insufficient d. Can't say

19. A 6-to-64 decoder can be obtained by cascading of _____

    a. Four numbers 4-to-16 decoders and one 2:4 decoder b.Five numbers 4-to-16 decoders

    c.Three numbers 4-to-16 decoders and two 2:4 decoder d.Can not possible

20. EX-3 subtractor can be implemented by using _____ no of parallel adders

    a. 1 b. 2 c. 3 d. 4

6.4.4.3 TUTORIAL TOPICS

1. Give the schematic circuit for a BCD-to-decimal decoder. Give the truth-table for the same.

2. A combinational circuit is specified by the following two Boolean functionsDesign the circuit with a decoder and basic gates.

$$F = \Sigma m (1,5,9,15), G = \Sigma m (0,1,9,10,12)$$

6.4.4 UNIT-V

6.4.5.1 DESCRIPTIVE QUESTIONS

1. Implement the following boolean functions using PLA.

   f1(w,x,y,z) = P(0,1,3,5,9,13) , f2 (w,x,y,z) = P(0,2,4,5,7,9,11,15).

2. The following memory units are specified by the no of words times the number of bits per word. How many address lines and input-output data lines are needed in each case?

   i. 4K × 16 ii. 2G × 8 iii. 16M × 32 iv. 256K × 64. Give the number of bytes stored in the memories listed above.

3. (a) Draw the basic macro cell logic diagram and explain.

   (b) Explain the general CPLD configuration with suitable block diagram.

4. For a given 3-input, 4-output truth table of a combinations ckt, tabulate the PAL programming table for the ckt.

Inputs	Output
x y z	A B C D
0 0 0	0 1 0 0
0 0 1	1 1 1 1
0 1 0	1 0 1 1
0 1 1	0 1 0 1
1 0 0	1 0 1 0
1 0 1	0 0 0 1
1 1 0	1 1 1 0
1 1 1	0 1 1 1

ASSIGNMENT QUESTIONS

1. Tabulate the PLA programming table for the four Boolean functions listed below

   $A(x,y,z) = \Sigma(1, 2, 4, 6)$, $B(x,y,z) = \Sigma(0, 1, 6, 7)$ $C(x,y,z) = \Sigma(2,6)$ $D(x,y,z) = \Sigma(1, 2, 3, 5, 7)$.

2. Write a brief notes on
   a) Architecture of PLD's. b)Capabilities and limitations of threshold gates.

6.4.5.2 OBJECTIVE QUESTIONS

1. Information in a memory chip is stored in _____form.
   a. Binary b. Decimal c. Hexadecimal d. Octal
2. The maximum number of bytes which can be stored in a memory of size 1024*8 is _____.

a. 64 b. 256 c. 1024 d. 2k

3. A shift register is a _____ memory.
   a. Parallel access b. Serial access c. both d. none
4. PLA is comprised of programmable_____ arrays.
   a.AND b.AND and OR c.OR d. None
5. PAL is comprised of programmable_____ gates.
   a OR b. NAND c. NOR d.AND
6. An ASIC is configured by the _____
   a Programmer b. Manufacturer c. Dealer d. none
7. A PAL has 10 input pins, the number of inputs to each of the AND gates is _____
   a.10 b. 20 c. 30 d. 40
8. Input buffers in PLA and PAL devices have _____ outputs.
   b. Inverting b. Non-Inverting c Inverting and non-inverting d. none
9. In a PLD, an _____ is provided for programming the polarity of the output.
   a. EX-OR b. OR c. AND d. NOR
10. A _____ is incorporated between the OR gate and output buffer in a registered PAL.
    a.T-FF b.SR-FF c.JK-FF d.D-FF
11. For maximum possible security of the digital circuit _____ design is preferred.
    a. ASIC b. MOS c. CMOS d.none
12. For designing digital circuits of the complexity of a few hundreds of gates _____ is preferred.
    a. PAL b.ROM c.PAL d.PROM
13. The number of address lines required in a memory of 128K*8 is _____
    a.15 b.8 c.16 d.17
14. The number of IC chips of memory size 1024*4 required to have 16K*8 memory will be ____
    a.16 b.8 c.4 d. 32
15. While specifying the memory size, the letter K stands for _____
    a.1000 b.64 c.1024K b.1024
16. A dynamic RAM is fabricated using _____ technology.
    a.CMOS b.ASIC c.MOS d.none
17. A serial EEPROM has _____ input/output.
    a.serial b.parallel c.both d.none
18. The FIFO memory has _____ ports.
    a.1 b.2 c.3 d.4
19. A FIFO memory can be used as a _____ buffer.
    a. Bidirectional b. Unidirectional c. Omnidirectional d. none
20. The burst feature in a synchronous SRAM _____ its speed.
    a.decreases b.increases c.double d.quadraple

6.4.5.3 TUTORIAL TOPICS

1. Derive the PLA programming table for the combinational circuit that squaresa 3 bit number.

2. Tabulate the PLA programming table for the four Boolean functions listed below

A(x,y,z) = ε(1, 2, 4, 6) B(x,y,z) = ε(0, 1, 6, 7) C(x,y,z) = ε(2,6) D(x,y,z) = ε(1, 2, 3, 5, 7).

6.4.6 UNIT-VI

6.4.6.1 DESCRIPTIVE QUESTIONS

1. (a) Using a shift register, how do you obtain a circular shift?

   (b) What is the principle used to convert an even modulo counter into an odd modulo counter?

2. (a) Draw the logic diagram of a 4 bit binary ripple counter using positive edge triggering.

   (b) Draw the block diagram of a 4 - bit serial adder and explain its operation.

3. Draw the logic diagram of a SR latch using NOR gates. Explain its operation using excitation table.

4. Show that the characteristic equation for the complement out put of a JK flipflop is
   Q′ (t + 1) = J ‘Q′ + kQ.

ASSIGNMENT QUESTIONS

1. Design Mod-6 synchronous counter using JKFF’s.
2. Explain the following
   a. Race around condition in FF’s.b) JK master slave FF. c)Excitation table for FF’s.

6.4.6.2 OBJECTIVE QUESTIONS

1. Flipflop is a _____ element.

   a.storage b.memory c.both d.none

2. Number of FF’s required for storing n-bit information is _____

   a.1b.4 c.2n d.n

3. In a SR FF, if S=R=1 _____.

   a.0b. 1 c.toggle d. Is not permitted

4. Preset and Clear inputs are used in a FF for making Q=____ and _____ resply.

   a.0,1 b.1,0 c.1,1 d.0,0

5. In a JK FF if J=K=1, its Q output will be _____ when clock pulse is applied.

   a.Q b.Q^1 c.0d.1

6. Master slave configuration is used in a JK FF to eliminate _____

   a.toggling b.clock c.preset d.race around

7. In a T FF, The Q output _____ when T=0 and clock pulse is applied.

   a.0b.1 c.togglesd.does not change

8. A FF has _____states.

   a.2b.3 c.4d.6

9. A latch is used to store 1 ____ of data.

   a.byte b.bit c.word d.doubleword

10. The negative edge triggered FF changes state at the_____ of the clock
    a.pulse.falling edge b.trailing edge c.both d.none

11. An active low Clear input clears the FF when it is _____

    a.low b.high c.constant d.none

12. A FF with active low preset input will have Q^1=_____ when preset is connected.

    a.1b.0 c.toggle d.none

13. The tabulation specifying inputs required for a FF to change from the present state to a specified next state is known as _____

    a.truth tableb.excitation table c.both d. None

14. Registers and counters can be designed using _____

    a.FlipFlop's b.gates c.both d. none

15. The minimum no of FF's required for a decade counter _____

    a.1 b. 2 c. 3 d.4

16. Race condition may exist in _____ sequential circuits.

    a.asynchronous b. Synchronous c. Both d.none

17. The modulo of a 4 bit binary counter is _____

    a.4b.8 c.16 d.32

18. A ripple counter is a _____ sequential circuit.

    a.asynchronous b. Synchronous c. Both d.none

19. The modulo of a 4 stage twisted ring counter is _____

    a.2b.4 c.8d.16

20. A 3 bit synchronous counter can be converted to a mod-8 ring counter by using _____

    a. 3-to-8 decoder b. 3-to-8 encoder c. 3-to-8 mux d.3-to-8 demux

6.4.6.3 TUTORIAL TOPICS

1. Design a sequence detector which detects 110010 Implement the sequence detector by using D - type flipflops.
2. Discuss about the FF's and their truth tables and excitation tables.

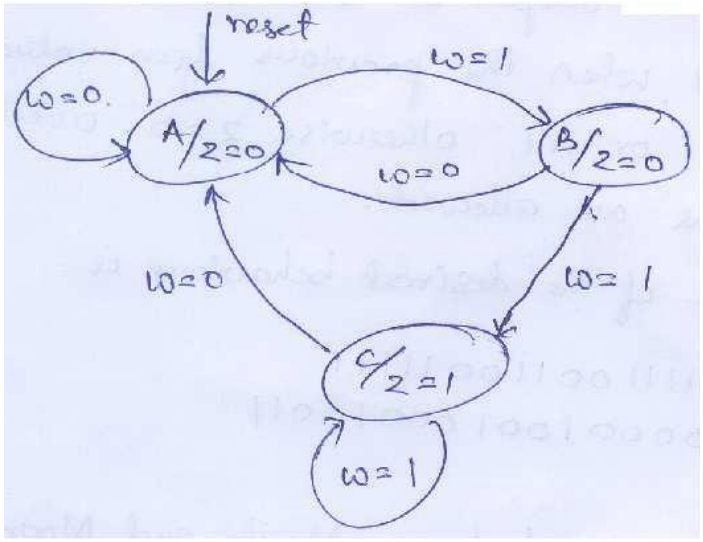
6.4.7 UNIT-VII

6.4.7.1 DESCRIPTIVE QUESTIONS

1. Explain the following related to sequential ckts with suitable examples.

   (a) State diagram (b) State table (c) State assignment.

2. Find the state table for the following state diagram



3. Draw the diagram of mealy-type FSM for serial adder.
4. (a) Draw the ckt for the moore type FSM.

   $x1(P,Q,R) = \Sigma(0,1,2,7)$, $x2(P,Q,R) = \Sigma(1,4,5,6)$.

   (b) Explain merger chart methods of minimal cover table.

ASSIGNMENT QUESTIONS

1. A clocked sequential circuit is provided with a single input x and single output Z.Whenever the input produce a string of pulses 1 1 1 or 0 0 0 and at the end of the sequence it produce an output

Z = 1 and overlapping is also allowed.

(a) Obtain State - Diagram. (b) Also obtain state - Table. (c) Find equivalence classes using

partition method & design the circuit using D- flip-flops.

2.A Clocked sequential circuit with two inputs x and y and a single output Z is defined by the

following J - K flip-flops state equations and output equation of Z.

$Q^{+}1 = Q1\ x^{1} + Q1\ y + Q2\ x + (Q1Q2)^{1}y^{1}$, $Q^{+}2 = (Q1)^{1}Q2\ x^{1} + (Q1)^{1}Q2\ y + (Q1Q2)^{1}\ x$

$$Z = (Q1 + Q2)\ (xy)^{1}$$

Where Q+1 ξQ+2 are the next states and Q1ξQ2 are the present states of J & Kflip-flops.

(a) Derive state - table. (b) Derive input equations. (c) Derive state - diagram.

6.4.7.2 OBJECTIVE QUESTIONS

1. In _____ machine, the output is a function of the present state and present inputs.

a.moore b.mealy c.both d.none

2. In _____ machine, the output is a function of only the present state

a.moore b.mealy c.both d.none

3. The sequence of inputs, present state and the next states and the outputs can be represented by ____

a. state table b. State diagram c.both d. None

4. A vertex is a _____ vertex if there are no outgoing arcs which emanate from it and terminate in

other vertices.

a. source b. sink c. terminal d. none

5. A 3 input sequential circuit will have _____ no of arcs emanating from a state.

a. 8 b.4 c.2 d.1

6. In a state diagram if a directed arc terminates on the same node from which it has emanated , the

next state will be_____

a. output b. carry c. input d. same as present state

7. In a state table containing 4 rows, the number of states is _____

a.1 b.2 c.4 d.8

8. 0/1 written by the side of the directed arc in a state diagram indicates 0 ____ and 1 _____

a. input, output b. output, input c. output, next state d. input, present state

9. A minimum no of _____ changes must occur in the output corresponding to dynamic hazard.

a.1 b.2 c.3 d.4

10. A minimum of _____ paths must exist between an input variable and output for dynamic hazard

to occur.3

a.1 b.2 c.3 d.4

11. The maximum possible number of states in a clocked sequential circuit having 5 FF's is ____

a.4 b.8 c.16 d.32

12. If an input sequence y-takes a machine from state A to B then B is said to be _____ of A.

a.y-successor b. Y-equivalent c. Y-distinguishable d.all

13. Minimization of the no of states reduce the _____

a.complexity b. No of gates c. Cost d.all

14.The state reduction process in the incompletely specified machines can be done by

a.merger graph b.merger table c.both d.none

15.Two compatible state pairs in the merger graph are indicated by _____

a.undirected arc b. Arc with implied pair c. No arc d.none

16.The compatibility of two states pairs in the merger table are indicated by

a. X-mark b. tick mark c. empty d. implied pair

17.If two states A and B, of a machine M are distinguishable, then they are distinguishable by a

sequence of _____ length.

a.(n-1) or less b.n or less c. n+1 d. does not depend on n

18.For a 8 state machine if P4=(A)(B)(CD)(EFG)(H), then its P3 partition may be _____

a.(CD)(A)(B)(EFG)(H) b.(AB)(CD)(EF)(GH) c.(AB)(CD)(EH)(FG) d.(ABC)(DEF)(GH)

19.Critical race must be _____ in a sequential circuit.

a. avoided b. necessary c. can't say d. none

20.The next state of a mealy machine is a function of _____

a. present state b. present input c. both d. none

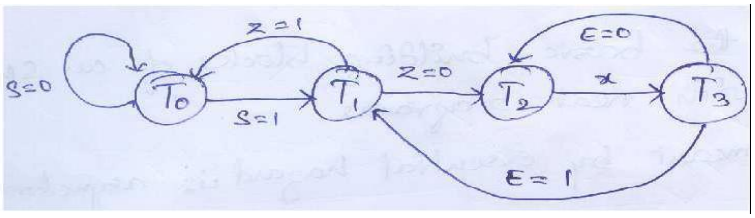
6.4.7.3 TUTORIAL TOPICS

1. A clocked sequential circuit is provided with a single input x and single output Z. Whenever the input produce a string of pulses 1 1 1 or 0 0 0 and at the end of the sequence it produce an output Z = 1 and overlapping is also allowed.
   (a) Obtain State - Diagram. (b) Also obtain state - Table.
   (c) Find equivalence classes using partition method & design the circuit using D- flip-flops.

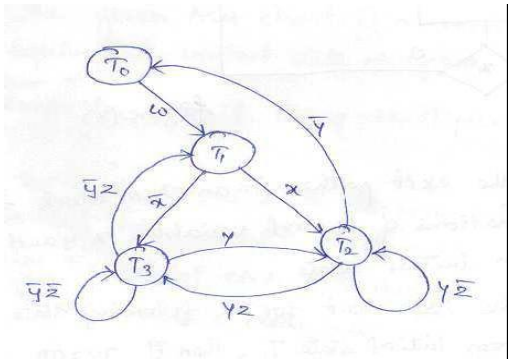
6.4.8 UNIT-VIII

6.4.8.1 DESCRIPTIVE QUESTIONS

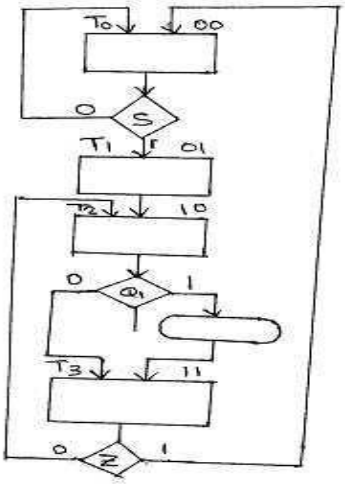
1. For the given state diagram, as shown in figure obtain its ASM chart and Design the above circuit using one flip flop per each state.



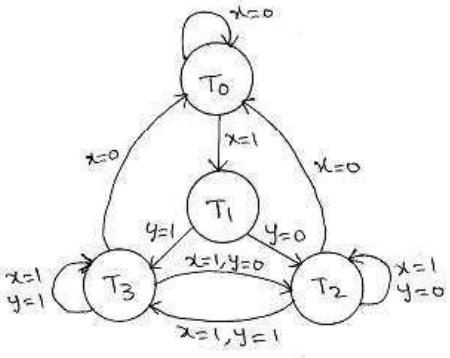
2. For the given control state diagram, draw the equivalent ASM chart and Design the control circuit using multiplexers



3. For the ASM chart given below, draw the state diagram and Design the control unit using D-flip flops and a decoder.



4. The state diagram of a control unit is



(a) Draw the equivalent ASM chart

(b) Design the control unit using D flip-flops and a decoder.

Assinment Questions

1. For the ASM chart given

(a) Draw the state diagram(b) Design the control circuit using multiplexers.

2.Draw the ASM chart for the following state transistion, start from the initial state T1, then if xy=00 go to T2, if xy=01 go to T3, if xy=10 go to T1, other wise go to T3.

6.4.8.2 OBJECTIVE QUESTIONS

1. The flow table of an asynchronous sequential circuit with 6 states and 2 inputs will have _____ rows and _____ columns.
   a.2,6 b.6,2 c.4,2 d.2,4

2. The speed of the asynchronous counter is _____ than that of the synchronous counter.
   a. lower b. higherc. can't say d. none

3. The number of the inputs which can change simultaneously in a fundamental mode asynchronous sequential circuit is _____
   a.4 b.2 c.1d.0

4. The number of the pulse inputs which are allowed to be present simultaneously in a pulse mode asynchronous sequential circuit is _____
   a.4 b.2 c.1d.0

5. An asynchronous sequential circuit consisting of NOR latch is required to be hazard free. Its inputs should be supplied from ___
   a. AND-OR b. NAND-NAND c. both d. none

6. An asynchronous sequential circuit consisting of NAND latch and OR-AND combinational circuit is _____
   a. hazards b. hazard free c. both d. none

7. Essential hazards cause _____ of an asynchronous sequential circuit.
   a. malfunctioning b. errors c. both d. none

8. An asynchronous sequential circuit with NOR latch is free of static _____ hazard.
   a.4b.3 c. 2 d.1

9. An asynchronous sequential circuit with NAND latch is free of static _____ hazard.
   a.4b.2 c. 1 d.0

10. Critical race must be _____ in an asynchronous sequential circuit.
    a. avoided b. necessary c. can't say d. none

11. An asynchronous sequential circuit reaches the same stable next state through two different paths in the flow table _____ race occurs in the critical circuit.
    a. critical b. Non- critical c. time critical d. none

12. _____ box is used to represent register operations.

    a. outputb. decision c. input d. state

13. _____ box is used to represent conditional outputs.

    a. output b. input c. decision d. state

14_____ box is used to represent unconditional outputs.

    a. output b. input c. decision d. state

15. The no of paths from a decision box is _____

    a.1 or more b.1 c.2 or more d.2

16. A simple ASM block contain only _____ box.

a.1 decision box b.2 decision box c. 1 state box d.2 state box

17. In one FF per state method, one FF is in _____condition and all other FF's are in _____

condition.

a. clear,clear b.set,set c.clear, set d.set, clear

18. In one FF per state method, _____ input of all FF's are connected common

a.clear b. set c. clock d.none

19. The no of MUX required to design the control logic of a 4 state problem is _____

a.1b. 2 c. 3 d.4

20. The design of control circuit with MUX is a _____ level implementation.

a.4b.3 c.2d.1

6.4.8.3 TUTORIAL TOPICS

1. Draw the ASM chart for the following state transistion, start from the initial state T1, then if xy=00 go to T2, if xy=01 go to T3, if xy=10 go to T1, otherwise go to T3.
2. Show the exit paths in an ASM block for all binary combinations of control variables x, y and z, starting from an initial state.

7.EM THEORYAND TRANSMISSION LINES

7.1 JNTUH SYLLABUS

UNIT I ELECTROSTATICS [1] : Coulomb's Law, Electric Field Intensity – Fields due to Different Charge Distributions, Electric Flux Density, Gauss Law and Applications, Electric Potential, Relations Between E and V, Maxwell's Two equations for Electrostatic Fields, Energy Density, Related Problems.

UNIT II Electro Statics II : Convection and Conduction Currents, Dielectric Constant, Isotropic and Homogeneous Dielectrics, Continuity Equation, Relaxation Time, Poisson's and Laplace's Equations; Capacitance – Parallel Plate, Coaxial, Spherical Capacitors, Related Problems.

UNIT III Magnetostatics : Biot-Savart Law, Ampere's Circuital Law and Applications, Magnetic Flux Density, Maxwell's Two Equations for Magnetostatic Fields, Magnetic Scalar and Vector Potentials, Forces due to Magnetic Fields, Ampere's Force Law, Inductances and Magnetic Energy. Related Problems.

UNIT IV Maxwell's Equations (Time Varying Fields) : Faraday's Law and Transformer emf, Inconsistency of Ampere's Law and Displacement Current Density, Maxwell's Equations in Different Final Forms and Word Statements. Conditions at a Boundary Surface : Dielectric-Dielectric and Dielectric-Conductor Interfaces. Related Problems

UNIT V EM Wave Characteristics – I : Wave Equations for Conducting and Perfect Dielectric Media, Uniform Plane Waves – Definition, All Relations Between E & H. Sinusoidal Variations. Wave Propagtion in Lossless and Conducting Media. Conductors & Dielectrics – Characterization, Wave Propagation in Good Conductors and Good Dielectrics. Polarization. Related Problems.

UNIT VI EM Wave Characteristics – II: Reflection and Refraction of Plane Waves – Normal and Oblique Incidences, for both Perfect Conductor and Perfect Dielectrics, Brewster Angle, Critical Angle and Total Internal Reflection, Surface Impedance. Poynting Vector and Poynting Theorem

UNIT VII Transmission Lines - I : Types, Parameters, Transmission Line Equations, Primary & Secondary Constants, Expressions for Characteristic Impedance, Propagation Constant, Phase and Group Velocities, Infinite Line Concepts, loss less ness/Low Loss Characterization, Distortion – Condition for Distortionlessness and Minimum Attenuation, Loading - Types of Loading. Related Problems.

UNIT VIII Transmission Lines – II : Input Impedance Relations, SC and OC Lines, Reflection Coefficient, VSWR. UHF Lines as Circuit Elements; $\lambda/4$, $\lambda/2$, $\lambda/8$ Lines – Impedance Transformations,significance of z_{min} and z_{max} smith Chart –Configuration and Applications, Single and Double Stub Matching. Related Problems.

TEXT BOOKS :

1. Elements of Electromagnetics – Matthew N.O. Sadiku, Oxford Univ. Press, 3rd ed., 2001.

2. Electromagnetic Waves and Radiating Systems – E.C. Jordan and K.G. Balmain, PHI, 2nd Edition, 2000.

3. 5. Transmission Lines and Networks – Umesh Sinha, Satya Prakashan (Tech. India Publications),New Delhi,

REFERENCES :

1. Engineering Electromagnetics – Nathan Ida, Springer (India) Pvt. Ltd., New Delhi, 2nd ed., 2005.

2. Networks, Lines and Fields – John D. Ryder, PHI, 2nd ed.,1999.

3. Engineering Electromagnetics – William H. Hayt Jr. and John A. Buck, TMH, 7th ed., 2006.

7.2 UNIT WISE PLANNER FOR ACADEMIC YEAR 2013 - 2014
Subject: EM WAVES AND TRANSMISSION LINES

Unit No.	Date Planned to complete	Date Conducted	Remarks
I			
II			
III			
IV			
V			
VI			
VII			
VIII			

7.3 SESSION PLANNER

S.No	Unit No	Topic	Date Planned	Date Conducted	Remarks
1.	I	Introduction to vector algebra & calculus			
2.		Coordinate system & Transformations of coordinate system			
3.		Coulomb`s law statement			
4.		Field intensity			
5.		Fields due to continuous charge distribution			
6.		Electric flux density			
7.		Gauss law & Applications			
8.		Electric potential ,Relations b/w E & V Maxwell's equation			
9.		Energy Density in electro static fields			
10.		Numericals			
11.	II	Convection &conduction currents			
12.		Continuity equ, Relaxation time			
13.		Isotropic & Homogeneous dielectrics			
14.		Conductors, dielectric constant			
15.		Poisons & laplace's equation			
16.		Capacitance, parallel plate capacitor			
17.		Coaxial, spherical capacitor			
18.		Numericals on poisons & laplace's equs			
19.	III	Biot-savart law statement			
20.		Amperes ckt law &Applications			
21.		Magnetic flux density,Maxwell's equs			
22.		Magnetic scalar & vector potentials			
23.		Force due to magnetic fields			
24.		Ampere's force law			
25.		Inductance & Magnetic energy			
26.		Numericals			
27.	IV	Faradays law &Transformater			

		e.m.f			
28.		Inconsistency of Amperes law			
29.		Displacement current density , Maxwells equqtion different forms			
30.		Boundary Conditions Dielectric-Dielectric			
31.		Dielectric-conductor interfaces			
32.		Maxwell's equ in word statements & Numerical			
33.	V	Wave equations for conducting media			
34.		Uniform Plane waves, Relations b/w E&H			
35.		Wave propagation in loss less media			
36.		Wave propagation in Dielectrics			
37.		Wave propagation in conductors			
38.		Good Dielectrics			
39.		Polarization, Numerical			
40.	VI	Reflection & Refraction of plane waves for Normal incidences & oblique incidences			
41.		Normal incidences for perfect Conductors			
42.		Normal incidences for perfect Dielectrics			
43.		Brewster Angle & Critical Angle			
44.		Surface impedance & internal Reflection			
45.		Poynting vector Theorem			
46.		Applications of Theorem			
47.		Power loss in a plane conductor & Numerical			
48.	VII	Transmission line types, Parameters of Tx lines			
49.		Line equations of Tx lines			
50.		Primary & second constants			
51.		Exp for characteristic impedence			
52.		Propag. Const,phase gnd velocities			
53.		Line concepts ,loss less/low loss			
54.		Condition for distortion less & minimum attenuation			
55.		Types of loading, Problems			

56.		Input impedance Relation of Tx line			
57.	VIII	SC & OC lines			
58.		Reflection coefficient			
59.		VSWR,VHF lines			
60.		Impedance Transformation			
61.		Smith chart			
62.		Configuration & Applications			
63.		Single & double stab matching			
64.		Transmission lines			

7. 4. QUESTION BANK

7.4.1 UNIT-I

13.4.1.1 DESCRIPTIVE QUESTIONS

1.Using Gauss's law derives expressions for electric field intensity & flux density?

2.State & explain coulomb's law?

3.Point charge 5 nc and -2 nc are located at (2,0,4) and (-3,0,5),respectively. Determine the force on a 1-nc point charge located at (1,-3,7).

4.Point charge 5 nc is located at (-3, 4,0) while line y=1,z=1 carriers uniform charge 2 nC/m.If V=0v at O(0,0,0),find V at A(5,0,1).

ASSIGNMENT QUESTIONS

1.Using Gauss's law derive expressions for electric field intensity & flux density?

2. Define Electric potential & Maxwell's two equations for electrostatic fields?

7.4.1.2 OBJECTIVE QUESTIONS

1 . Four equal magnitude positive charges,' Q' each are placed at four corners of a square with the

centre of the square at origin. The net force on a point charge, Q2 placed at origin with E0 = Q *Q

$2 / (4 \pi \epsilon_0 R^2)$ s

(a) $2\sqrt{2}$ E 0 (b) 4 E 0 s i n θ (c) 4 E 0 (d) z e r o

2 . The field intensity due to a line charge plate distance of 1cm is E1 = 1V/m. The electric field

intensity E2 at a distance of 2cm from another line of density ty the at is four times that of ρl

(a) 2 V /m (b) 0 . 5 V /m (c) 1 V /m (d) 4 V /m

3 . Value of proportionality constant of Coulomb's law is

a) 9 × 1 0 9 m / F (b) 8 . 8 54 × 1 0 1 2 F / m (c) 1 3 6 π × 1 0 9 m / F (d) 9 × 1 0 - 9 F / m

4 . According to Coulomb's law, the force F between two point charges Q1 and Q2

(a) Directly proportional to product of Q21 and Q22

(b) is inversely proportional to the cube of the distance between them

(c) Is proportional to inverse of the square of the distance between them

(d) Is not along the line joining them

5. The flux density on a G Gaussian surface enclosing a sphere with uniform charge ρv C/m 3 and radius a

is given by

(a) a 3 3 r 2. ρv a r (b) 4 π r ρv3 . a ρ (c) r 3 . ρ v a r (d) 4 r3 . ρ v a r

6. The field intensity due to a line charge ρl at a distance of 1cm is E1 =1V/m. The

Electric field intensity E2 at a distance of 2cm from another line of density that is four Times that of ρl

(a) 2 V /m (b) 0 . 5 V /m (c) 1 V /m (d) 4 V /m

7.. Identify in correct statement

(a) For symmetrical charge d distributions , coulomb 's law them to provides convenient analysis compared to Gauss 's law (b) Gauss's law is an alternative statement of coulomb's law

(c) According to Gauss's law, electrical flux due to any closed surface is equal to the charge enclosed by the surface (d) Gauss's law states that ρV = ▼. D

8. Identify in correct statement

(a) Units of potential difference is Volts (b) Units of potential difference is Joule s /Coulomb

(c) The potential at any point is the potential difference between that point and t h e ori gin

(d) The potential difference between two point s A and B , V A B is independ ent of the path taken

9. J = σ E, describing Ohm's law cannot be applied to

(a) Isotropic media (b) Homogeneous media (c) Convection currents (d) Conduction currents

10. Exponential decay of charge density with time is based on the time constant T, referred to as

(a) Relaxation time e (b) Transit time (c) Relapse time e (d) Displacement time

11. Is Q1 and Q2

(a) Directly proportional to product of Q21 and Q22

(b) is inversely proportional to th e cube of the distance between them

(c) Is not along the line joining them

(d) Is proportional to inverse of the square of the distance between them

12. Identify incorrect statement

(a) Units of potential difference is Joules /Coulomb (b) Units of potential difference is Volts

(c) The potential l at any point is the potential a l difference between that point and the origin

(d) The potential a l difference between two points A an d B , V_{AB} is independent of the path taken

13. Identify the equation for potential that does not satisfy Lap lace's equation

(a) V = 10xy (b) V = (3y +1z) (c) V = (▼. x2 + y2) . Cos φ (d) V = (2x +5)

14. If the magnetic field H =10a_x A/m, the flux density in free space is

(a) 4 π a x μ W b / m 2 (b) 1 . 6 π a x μ W b / m 2 (c) 4 0 π a x μ W b / m 2 (d) 1 0 π a x μ W b / m 2

15. A wire of 1mm diameter with conductivity of 5 ×107mho/m has 1020 electrons per unit volume. The conduction current density for an applied field of 10mV/m is

(a) 5 00 k A /m 2 (b) 5 × 1 0 - 9 A / m 2 (c) 5 × 1 0 - 1 3 A / m 2 (d) 5 × 1 0 7 A / m 2

16. The electric flux density on a spherical su rfac er =b is the same for a point cha rge Q located at the origin and for a charge Q uniformly distributed on surface r =a (a < b)

(a) Both cases have nothing in common (b) True (c) Fals e (d) Not necessarily

17. Sea water has ▼ r = 80, the permittivity of sea water is

(a) 7.07×10-10 F / m (b) 1/80 (c) 80×10-10 F/m (d) 80 only

18. If the electric flux density, D and electric field intensity, E are not in the same directi on , the material is

called as

(a) An isotropic medium (b) Linear medium (c) An aniotropic medium (d) Homogeneous medium

19. If the field intensity is 1V/m due to a point charge Q1 at a distance of 1cm, the fie ld intensity at a distance of 2cm if the charge increased by 4 times is

(a) 2V/m (b) 1V/m (c) 4V/m (d) 0.5V/m

20. Units of magnetic flux density are

(a) Webers/meter (b)Henry /meter (c) Webers/meter^2 (d) Amperes/meter ^{2}

7.4.1.3. TUTORIAL TOPICS

1.Numerical on Coulomb's law, Gauss law, Electric intensity, Electric potential

7.4.2 UNIT-II

7.4.2.1 DESCRIPTIVE QUESTIONS

1. Write the difference between Isotropic and Homogeneous Dielectrics?

2. State Relaxation time, Poisson's and Laplace's equations?

ASSIGNMENT QUESTIONS

1. Write the difference between conduction and convection current & parallel plate capacitor and coaxial spherical capacitor?

2. Derive equation of continuity for static magnetic fields?

7.4.2.2 OBJECTIVE QUESTIONS

1. The constant of proportionality of Biot -Savart law is
   (a) 1/4π (b) 1/4π F/ m (c) 9 ×109 F/ m (d) 1/4 π A / m

2. Magnetic field in aToroid is

   (a) 1 2 π ρ (b) N I l (c) I ρ 2 π a 2 (d) N I 2 π r

3. Identify in correct statement

   (a) units of potential difference is Volt s

   (b) units of potential difference is Joules/Coulomb

(c) The potential at any point is the potential difference between that point and the origin

(d) The potential difference between two points A and B , VAB is independent of the path taken

4. Boundary Conditions on fields at an interface is given by

(a) E tan1= E tan2 (b) E tan1 = E n or m2 (c)E tan1 = H tan1 (d)E tan1=Hn or m 1

5. Inductance of long conductor wire is given by

(a) L = (μ_0 / π). l .l n (b/a) (b) L = μ_0l 2 π [l n (2 l a) - 1] (c) L =μ_0 N 2 S / l (d) L = μ o l / 8 π

6. Identify Maxwell's equation which is not applicable for static field s

(a) ▼ × E = 0 (b) ▼ × H = ∂ D ∂ t (c) ▼ × E = - ∂ B ∂ t (d) ▼ × H = J + ∂ D ∂ t

7. Identify Maxwell's equation which is not in phasor form

(a) ▼ × H = j w D + J (b) ▼ × E = - ∂ B ∂ t (c) ▼× E = - j w B (d) ▼× D = ρ v

8. Identity the in correct statement

(a) magnetic force between two current elements is equal to the field produced by Biot - Savarts l aw

(b) Between two current elements , the force is dependent on the magnetic field based on Biot - Savart s l aw

(c) Force between two current carrying conductors is not given by Lorentz 's Force Equation

(d) Force on a current carrying conductor is dependent on the magnetic field in which it is placed .

9. The unit of magnetic susceptibility is

(a) Henry/meter (b) No units (c) Amperes (d) Weber

10. Lorentz force equation is given by

(a) F= e(E+v ×B) (b) F= IL ×B (c) F= ev ×B (d) F=eE

11. Inductance of a conductor

(a) Has units of Webers/Ampere (b) Has units of Tesla/m^2 (c) Has units of Webers/Meters

(d) Has units of Amperes/meter

12 If a parallel plate capacitor connected to a bat tery, stores twice as much charge as wi th air diectric ,

the susceptibility of the dielect ric material between the capacitor plates is (a) 4 (b) 1 (c) 0 (d) 2

13. Identify in correct statement

(a) Biot -Savart' s and Ampere's laws , both are governing laws of electrostatics

(b) Similar to Coulomb's law , Biot -Savart's lawi s inverse square law of distance due to differential

current element (c)Ampere's law can also be applied to non symmetric current distribution s

(d) Magnetic field intensity due to a differential current element I d l at a distance ' R ' is proportional to

$1 / R^2$

14. Vector Magnetic Potential has units of

(a) Ampere/meter (b) Weber (c) Amperes (d) Webers/Meter

15. Lorentz force equation describes an expression for force

(a) on a current element I dl in a magnetic field (b)on a moving charge with a velocity v in a magnetic field

(c) on a stationary or moving electric charge in an electric field

(d)on a moving charge in elect ric and magnetic field s

16. Units of inductance are not give n by

(a) Weber/Meter (b) Webers/Ampere (c) Weber-sec/coulomb (d) Henry s

17. The equation, $\nabla . J = - \partial \rho v \partial t$ is referred to as

(a) Equation of continuity in integral form (b Equation of continuity in point form

(c) Helm holtz equation (d) Laplace equation

1 8. Identify the two equations indicating the inconsistency of ampere's law for time Varying fields

(a) $\nabla \cdot B = 0$ and $\nabla \cdot J = 0$ (b) $\nabla \cdot (\nabla \times H) = 0$ and $\nabla \cdot J = 0$ (c) $\nabla \times H = J$ and $\nabla \times E = - j w B$ (d) $\nabla \times H = J$ and $\nabla . J = \rho v$

19. For a dielectric -dielectric interface at the boundary,

(a) Tangential component of H is non-continuous by the amount of current density on

the interface . (b) Tangential component of H is continuous (c) Tangential component of E is not continuous (d) Tangential component of H is not continuous

2 0. Polarization of an E lectromagnetic wave is deifne as

(a) The direction of E ×H Vector . (b The direction of magnetic field vector.

(c The direction of the propagation of the Wave . (d The direction of Electric field vector .

7.4.2.3. TUTORIAL TOPICS

1 . Numerical on magnetic flux, magnetic scalar & vector potentials.

7.4.3 UNIT-III

1. **7.4.3.1 DESCRIPTIVE QUESTIONS** State Maxwell's equation for magneto static fields?
2. Define Magnetic scalar and vector potentials & Ampere's Force law?

3. Planes z=0 and z=4 carry current K=--10a_x A/m and K=10a_xA/m, respectively. Determine H at (a) (1,1,1) (b) (0,-3,10).

4. Given the magnetic vector potential A= -$\rho^2/4$ a_z wb/m, calculate the total magnetic flux crossing the surface $\Phi=\pi/2, 1< \rho<2m, 0<z<5m$.

ASSIGNMENT QUESTIONS

1. Explain magnetic flux density & State Maxwell's two equations for Magnetostatic fields?

2. Write about inductances and magnetic energy?

7.4.3.2 OBJECTIVE QUESTIONS

1. Faraday's law is represented by the Maxwell's equation given as

(a▼× E = - ∂ B ∂t (b) ▼× H = ∂ B ∂t + J (c) ▼× H = ∂ D ∂t + J (d) ▼ × H = ∂ D ∂t

2. Identify the two equations indicating the inconsistency of ampere's law for time varying fields

(a) ▼· (▼ × H) = 0 a n d ▼· J = 0 (b) ▼× H = J an d ▼.J = ρv (c) ▼· B = 0 and ▼ ·J = 0 (d) ▼ × H = J an d ▼ × E = - j w B

3. At a conductor interface with surface charge density

(a) Normal component of D is not continuous (b) Tangential component of H is continuous (c) Normal component of B is not continuous (d) Tangential component of E is not continuous

4. At a conductor - dielectric interface with dielectric as medium 2

(a) H t a n 1 - H t a n 2 = J s o n m e d i u m 1 s u rf ac e (b) E t a n 1 - E t a n 2 = Js on medium 2 surface (c) E t a n 1 - E t a n 2 = J s on medium 1 surface (d) H t a n 1 - H t a n 2 = J s on medium 2 surface

5. Exponential decay of ch arge density with time is based on the time constant T ,referred to as (a) Relaxation tim e (b) Transit tim e (c) Relapse time (d)Displacement time

6. For a Uniform plane wave E an d H are related to each other through

(a) $E_y/H_z = [\mu/€]^{1/2}$ (b) B =▼E and D = μ H (c) E = μ H (d) E × H is always ' 0 '

7. I ntrinsic impedance, η , of a conducting medium is given by

(a) √ μ € (b) j ω μ / € (c) 1 20 π (d) [j ω μ / (σ + J ω €)] $^{1/2}$

8. Identify in correct Statement

(a) As frequency increases, the impedance of a wave traveling in a good dielectric Medium decreases

(b) For a perfect dielectric $\alpha = \beta$ (c) For a good conductor $\eta = (j \omega \mu / \sigma)$ 1 / 2 (d) For a good conductor $\alpha = \beta$

9. If a wave has Ex and Ey magnitudes equal and 90^0 phase difference between them, The wave is said to be

(a) Horizontally Polarized (b) Un Polarized (c) Elliptically Polarized (d) Circularly Polarized

10. Identify the equation which is not Maxwell's equation for a static electromagnetic field in a linear homogeneous medium

(a) $\nabla . D = \rho v$ (b) $\nabla . B = 0$ (c) $\nabla 2 A = \mu 0 J$ (d) $\nabla \times D = 0$

11. In cylindrical co-ordinates, the equation, $\partial 2E \partial \rho 2 + 1 \rho E \partial \rho + \partial 2E \partial z 2 = 0$ denotes

(a) Poisson's equation (b) Helm holtz's equation (c) Laplace equation

(d) Maxwell s equation for electro static fields

12. At a conductor interface with surface charge density

(a) Tangential component of E is not continuous (b) Normal component of B is not continuous

(c) Tangential component of H is continuous (d) Normal component of D is not continuous

13. For a dielectric-dielectric inte rface at the boundary,

(a) Tangential component of H is continuous (b) Tangential component of E is not continuous

(c) Tangential component of H is not continuous

(d Tangential component of H is non-continuous by the amount of current density on the interface .

14. Identify the in correct statement

(a) Displacement current density is same for static fields and free space .

(b) Displacement current density is same as conduction current density for time Varying fields.

(c) Displacement current density is given by $\partial D \partial t$

(d) Displacement current density is always zero for static field s .

15. Boundary conditions are applicable

(a) To normal components of electric and magnetic fields

(b) Only to the tangential components of elect ric and magnetic fields

(c) Only to electric fields (d) Only to magnetic field s

16. Normal component of B is continuous at

(a) Dielectric - Dielectric interface only (b) Conductor-conductor interface only

(c) Dielectric - Conductor interface only (d) Any discontinuity

17. Value of permeability of free space is

(a) $4\pi \times 1\ 0^{-7}$ H/ m (b) $1.36\pi \times 1.07$ H/m (c) $4\pi \times 1.07$ H / m (d) $3\ .6\pi \times 1.07$ H/ m

18. The unit of magnetic susceptibility is

(a) Weber (b)Amperes (c) No units (d) Henry /meter

19. Force on a moving charge due to electric and magnetic fields is given by

(a) $F = e (E + v \times B)$ (b) $F = I L \times B$ (c) $F = ev \times B$ (d) $F = eE$

20. Magnetic energy stored in an inductor (L) ca rrying current (I) and placed in a Magnetic field of intensity H

is given by

(a) $W = 1\ 2\ LH^2$ (b) $W = 1\ 2\ HI^2$ (c) $W = 1\ 2\ LI^2$ (d) $W = 12\ IH^2$

7.4.3.3. TUTORIAL TOPICS

1. Numerical on Transformer EMF, Boundary Conditions

7.4.4 UNIT-IV

13.4.4.1 DESCRIPTIVE QUESTIONS

1. 1. State displacement current density?
2. State boundary condition in scalar form?
3. Obtain the integral from of Maxwell's equation from amperes circuital law in the generalized form?
4. Explain Faradays law for time varying fields?

ASSIGNMENT QUESTIONS

1. Faraday's Law & transformer emf equation for time varying fields?

2. Explain about Inconsistency of Ampere's Circuit law?

7.4.4.2OBJECTIVE QUESTIONS

1.The Condition differentiating a good conductor from a good dielectric is

(a) (σ / ω μ) = 1 (b) σ / ω μ > > 1(c) σ / ω μ ≤ 1 (d) σ = (ω μ / 2) 1 / 2

2. Sea water has ▼r = 80 , the permittivity of sea water is

(a) 7 . 0 7 × 1 0 - 1 0 F / m (b) 8 0 × 1 0 - 1 0 F / m (c) 8 0 on l y (d) 1 / 8 0

3. Identify the NON Polarization term.

(a) Linear Polarization (b) Surface Polarization (c) Circular Polarization (d) None

4. Identify the equation for potential tha t does not satisfy Laplace's equation

(a) V = (2 x + 5) (b) V = (3 y + 10 z) (c) V = 1 0 x y (d) V = ▼ (x 2 + y 2) . c o s φ

5. The magnetic field at a point ρ distance away in the normal direction to an infinite current element is

given by (a) H = I 4 π ρ (c o s α 2 - c o s α 1) a φ (b) H = I 4 π ρ a φ (c) H = I 2 π ρ a φ

(d) H = I dl s i n φ 4 π ρ 2 . a φ

6. At a conductor interface with surface charge density

(a) Tangential component of E is not continuous (b) Tangential component of H is continuous

(c) Normal component of D is not continuous (d) Normal component of B is not continuous

7.At a conductor – dielectric interface with dielectric as medium 2

(a) E t a n 1 - E t a n 2 = J s on medium 2 surface (b) H t a n 1 - H t a n 2 = J s on medium 2 surface

(c) H t a n 1 - H t a n 2 = J s on medium 2 surface (d) E t a n 1 - E t a n 2 = J s on medium 2 surface

8. Solution for a Uniform plane wave in free space is traveling in positive x direction is

(a) E = f (x)+f(t)+f(y) (b) E = Ex =constant (c) E =f (x +v0(t)) (d) E = f (x - v0(t))

9. Units of magnetic field intensity are

(a) A m p e r e s /m e t e r (b) We b e r s / m e t e r (c) A m p e r e s (d) We b e r s

10. Identify a non - example of convection current

(a) current flowing in vacuum (b) current flowing in copper rod (c) electron beam in a TV tube

(d) current through inert gases

11. Identify polarisation which is not of similar type compared to the other three.

(a) Horizontal Polarisation (b) Vertical Polarisation (c) Linear Polarisation (d) Circular Polarisation

12. Inductance of a co-axial conductor is given by

(a) $L = \mu_o\ l\ 2\pi\ [\ l n\ (\ 2 l\ a\ ) - 1\ ]$ (b) $L = (\ \mu_o\ /\ \pi\ ) . l .\ l n\ (\ b / a\ )$ (c) $L = \mu_o\ N\ 2\ S / l$ (d) $L = \mu_o\ l / 8\pi$

13. For a uniform plane wave traveling along x - direction ,

(a) Ez = Hz = 0 (b) Ex = Ey = Hx = 0 (c) Ey = Hy =0 (d) Ex =Hx = 0

14.Identify in correct statement

(a) For symmetrical charge d distributions , coulomb 's law them to provides convenient analysis compared

to Gauss 's law

(b) Gauss's law is an alternative statement of coulomb's law

(c) According to Gauss's law, electrical flux due to any closed surface is equal to the charge enclosed by

the surface (d) Gauss's law states that $\rho V = \nabla . D$

1 5. For a medium if $\omega j << \sigma$, then the medium is

(a) a good conductor (b) a lossless medium (c) a good dielectric (d) Free Spa e .

16. Identify the non- Polarisation term

(a) Surface Polarisation (b) CircularPolarisation (c) Vertical Polarisation (d) Linear Polarisation

1 7. The constant of proportionality of Biot-Savart law is

(a) $1 / 4\pi$ (b) $1 / 4\pi$ F / m (c) $9 \times 1\ 0\ 9$ F / m (d) $1 / 4\pi$ A / m

18. Identify in correct statement

(a) In good dielectrics , electric flux density is larger than electric field intensity

(b) Electric fluxdensity is equal to Electric field intensity in air

(c) Electric fluxdensity is also referred to as Electric displacement

(d) Electric fluxdensity is also generally denoted by ψ

1 9. If $j\omega >> \sigma$ for a medium, then it is

(a) a good dielectric (b) a good conductor (c) Free Space (d) aloss less medium

20. Identify in correct statement for a plane wave travelling in a loss less medium

(a) At tenuation constant of free space is zero .

(b) The characteristic impedance , of a plane wave in loss less medium $\eta = 20\Pi$ Oh ms

(c) The characteristic impedance , η , of a plane wave in loss less medium is $\eta = \blacktriangledown (j \omega \mu) / (\sigma + j \omega)$

(d) The Propagation constant is purely imaginary.

7.4.4.3. TUTORIAL TOPICS

1.Numerical on Dielectric media, E & H, Conductors & Dielectrics

7.4.5 UNIT-V

7.4.5.1 DESCRIPTIVE QUESTIONS

1.For good dielectrics derive the expression for α,β,η and γ?

2.In a loss less medium for which $\eta=60\ \pi$, $\mu_r=1$, and H= -0.1c0s $(\omega t-z)a_x$ +o.5 $\sin(\omega t-z)a_y$ A/m,calculate ω,E and ϵ_r.H.

3.For the copper coaxial cable ,let a=2mm,b=6mm and t=1mm.calculate the resistance of 2m length of cable at dc and at 100MHZ.

ASSIGNMENT QUESTIONS

1. Define uniform plane waves & write all the relations between E & H?
2. Explain about wave propagation in lossless and conducting media?

7.4.5.2 OBJECTIVE QUESTIONS

1. Wave is a function of [b]

a) Both time & amplitude b Both space & time c. Both frequency & amplitude d. None

2. Among the following which one is used to measure of the depth to which an EM wave can penetrate the medium? [a]

a) Skin depth b) Galvanometer c) Both a & b d) None

3. What is the equation of standing wave ratio? [b]

a).1-γ/1+ γ b)1+ γ/1- γ c) 1- γ d) 1+ γ

4. What is the definition of Snell's law? [b]

a) Ndfl;$F_1 \sin\theta = n_2 \sin\theta$ b) $n_1 \sin\theta i = n_2 \sin\theta_t$ c) $n_1 \sin\theta_i / n_2 \sin\theta_t$ d) $n_1 \sin\theta i * n_2 \sin\theta_t$

5. The Brewster angle is also knowns as [c]

a) Incident angle b) Reflected angle c) Polarizing angle d) None

6. Exponential decay of charge density with time is based on the time constant T, referred to as

a) Relaxation time b) Transit time c) Relapse time d) Displacement time

7. The unit of scalar magnetic potential is

a) Ampere b) Volt c) Volt /meter d) Ampere/meter

8. For a dielectric - dielectric boundary interface

a) Normal component of both E and H are continuous b) Normal component of H is not continuous

c) Normal component of E is not continuous d) Normal component of H is discontinuous by the

surface charge density

9. If a wave has Ex and E_y magnitudes equal and 90^0 phase difference between Them, the wave i s said to be

a) Un Pola rised b) Elli ptically Polarised c) Circularly Pola rised d) Horizont ally Polarised

10. What are the units of *Skin Resistance* [a]

(a) Ω/m^2 (b) Ω (c) $1/\Omega$ (d) $\Omega/2$

11. When a wave is travelling from one medium to another medium, it is [b]

a).completely, transmitted b).partly, transmitted c).completely, refracted d).none

12. The reflection coefficient when a ave is normally incident from one medium to another medium is [d]

a).n_2+n_1/ n_2-n_1 b).$2n_2/ n_2-n_1$ c) $_{2n1}/ n_2+n_1$ d). n_2-n_1/ n_2+n_1

13. The relation between Ł and Π at normal incidence is [a]

a). $1+\Pi = Ł$ b). $\Pi = Ł$ c). $1+Ł = \Pi$ d). $Ł = \Pi+2$

14. The limits of Π are [b]

a.(0,1) b. [0,1] c.[0,1) d.(0,1]

15. In the case of normal incidence when $\sigma_1=0$ and $\sigma 2=\infty$ then wave is [c]

a). totally transmitted b).grazing the line between the media

c).totally reflected d).none

16. In the above case, when the wave is totally reflected [c]

a) Π=1 b). Π=0 c).Π=-1 d). Π=0.5

17. Sin Φ_t/sin Φ_i= [d]

a).$k_{i=}/k_t$ b).μ_2/μ_1 c). $[\mu_1\varepsilon_1/\mu_2\varepsilon_2]^{1/2}$ d).all

18. In the case of parallel polarization at oblique incidence the reflection coefficient is given by [a]

a). Π11=$2n_1\cos\theta_t/n_2\cos\theta_t+n_1\cos\theta_i$ b). $\Pi_{11}=2n_1\cos\theta_i/n_2\cos\theta_t+n_1\cos\theta_i$

c). $\Pi_{11}=2n_2\cos\theta t/n_2\cos\theta_t-n_1\cos\theta_i$ d).none

19. The Brewster angle in the case of parallel polarization oblique incidence when both the dielectric

media are not only loss less but non magnetic as well i.e.,$\mu_1=\mu_2=\mu_0$ [d]

a). $\sin^2\theta\beta_{11}=1/(1+\varepsilon_1/\varepsilon_2)$ b).tan $\theta\beta_{11}=\sqrt{\varepsilon_2/\varepsilon_1}$ c**).** tan $\theta\beta_{11}=n_2/n_1$d). All the above

20. Polarization of the wave is [b]

a). Parallel b).perpendicular c).either a or b d).none

7.4.5.3. TUTORIAL TOPICS

1.Numerical on Plane waves, pointing theorem

7.4.6 UNIT-VI

7.4.6.1 DESCRIPTIVE QUESTIONS

1. Define & derive expression for Brewster angle & critical angles?
2. An EM wave travels in free space with the electric field component

   $E_s=100\ e^{j(0.866y+0.5z)}a_x$ V/m. Determine the magnetic field component, the time average power in the wave, ω and λ.

3.. Write short notes on the following

a)surface impedance b) Total Internal Reflection

ASSIGNMENT QUESTIONS

1. Derive the expression for Brewster angle when a wave is parallel polarized?
2. State Poynting vector & pointing theorem?

7.4.6.2 OBJECTIVE QUESTIONS

1. In a transmission line terminated with a load equal to the characteristic impedance, the reflection coefficient is
   a)+1 b)λ/2 c)0 d) λ
2. Short circuited stubs are preferred to open-circuited stubs because the latter are
   a) more difficult to make and correct b) made of a transmission line with a different Z_o
   c) liable to radiate d) incapable of giving a full range of reactance
3. Decibel is a logarithmic unit expressing
   a) noise levels b) current c) voltage d) power ratio

4. Input impedance of a shorted lossless line of length λ / 4 is
   a) 0 b) 1 c) Z_o d) λ

5. Electromagnetic waves are reflected back by ionosphere due to their interaction with
   a) Electrons d) Protons c) Ultra-violet rays d) Neutrons

6. For a transmission line with λ L << R and λ C << G, attenuation constant λ is
   a) proportional to frequency b) constant c) inversely proportional to frequency d) proportional to velocity

7. When power ratios are expressed in dbm, the reference power is
   a) 1 W b) 1 mW c) 1 λ W d) 1 MW

8. In a distortion less line, attenuation constant is
   a) directly proportional to frequency b) inversely proportional to frequency
   c) independent of frequency d) independent of primary constants

9. Loading is used in cables to
   a) reduce distortion b) increase power handling capacity c) increase load resistance d) increase distortion

10. Input impedance of an open circuited loss-less line of length λ is
    a) infinity b) finite capacitive reactance c) finite inductive reactance d) zero

11. If the spacing between the wires of a transmission line is increased, its characteristic impedance will
    a) increase b) decrease c) is unchanged d) none
12. The reflection coefficient on a lossless transmission line
    a) is always purely imaginary b) is always purely real c) is always complex d) can be anyway

13. There will be no reflection in a transmission line if it is terminated by an impedance
   a) equal to characteristic impedance b) less than the characteristic impedance
   c) equal to twice the characteristic impedance d) equal to square root of its characteristic impedance

14. Among the following lines, the simplest one to construct is
a) strip line b) microstrip line c) coaxial cable d) optical fiber

15. The unit of magnetic field of electromagnetic radiation at any point is usually expressed in
a) ampere/meters b) volts/meter c) watts/meter d) watt/metre^2

16. The intrinsic impedance of free space is
a) 50 ohms b) 377 ohms c) 73 ohms d) 83 ohms

17. The velocity of electromagnetic waves in a dielectric ($\lambda = 4$) is
a) 3 x 108 m/sec b) 1.5 x 108 m/sec c) 6 x 108 m/sec d) 2 x 108 m/sec

18. The induction field of a short current element varies as?
19. The guide wavelength in a rectangular waveguide in TE10 mode is
a) greater than free-space wavelength b) less than free-space wavelength
c) equal to free-space wavelength d) double the free-space wavelength

20. VSWR in a short-circuited line equals
a) infinity b) unity c) zero d) none

7.4.6.3. TUTORIAL TOPICS

1.Numerical on Waveguides

7.4.7 UNIT-VII
7.4.7.1DESCRIPTIVE QUESTIONS

1. Write short notes on Loss less Transmission line?

2. List out the types of transmission lines and draw their schematic diagrams?

3. Draw the directions of electric and magnetic fields in parallel polarization?

4. Starting from the equivalent circuit, derive the transmission line equations for V, I, in terms of the source?

ASSIGNMENT QUESTIONS

1.Derive the expression for characteristic equation?

2. Define and explain the significance of the following terms as applicable to parallel plane guides a. wave impedance b. phase and group velocities

7.4.7.2 OBJECTIVE QUESTIONS

11. Define group velocity?

2. For electromagnetic waves traveling in free space, the power carried by the waves changes with distance $\lambda d\lambda$ in proportion to
a) d b) 1/d c) 1/d2 d) d2

3. What are the characteristics of TEM waves?

4. Electromagnetic waves are reflected back by ionosphere due to their interaction with
a) Electrons d) Protons c) Ultra-violet rays d) Neutrons

5. What is the cut off frequency of TEM wave?

6. The velocity of electromagnetic waves in a dielectric (λ= 4) is
a) 3 x 108 m/sec b) 1.5 x 108 m/sec c) 6 x 108 m/sec d) 2 x 108 m/sec

7. Give the expression that relates phase velocity (V_p), Group velocity (V_g) and free Space velocity?

8. The guide wavelength in a rectangular waveguide in TE10 mode is
a) greater than free-space wavelength b) less than free-space wavelength
c) equal to free-space wavelength d) double the free-space wavelength

9. What are TE waves or H waves?

10. The dominant mode in a cylindrical wavelength is
a) TM11 b) TE11 c) TE10 d) TM10

11. The MKS unit for λ is
a) farads per square metre b) farads per metre c) henrys per metre d) henrys per square metre

12. What are TM waves or E waves?

13. If the frequency is 10 MHz, the wavelength of a plane electromagnetic wave in free space will be
a) 30 metres b) 100 metres c) 60 metres d) 90 meters

14. The velocity of EM waves in free-space with respect to that in an RF cable with air dielectric is
a) increased b) decreased c) unchanged d) none

15. What are guided waves?

16. In a rectangular waveguide, the phase velocity
a) increase with increasing frequency b) decrease with increasing frequency
c) is independent of frequency d) none of these

17. The intrinsic impedance of free space is
a) 50 ohms b) 377 ohms c) 73 ohms d) 83 ohms

18. On a transmission line withstanding waves, the distance between a voltage maxima and adjacent current maxima is
a) λ / 4 b) λ / 8 c) λ / 4 d) λ

19. The velocity of EM waves in free-space with respect to that in an RF cable with air dielectric is
a) increased b) decreased c) unchanged d) none

20. A rectangular waveguide is
a) resonant circuit b) high pass filter c) low pass filter d) band pass filter

7.4.7.3. TUTORIAL TOPICS

1.Numerical on Transmission lines

7.4.8 UNIT-VIII

7.4.8.1 DESCRIPTIVE QUESTIONS

1. Define the reflection coefficient & derive the expression for the input impedance in terms of reflection coefficient?

2. A dipole antenna is fed by a transmission line having Z_o=60Ω.The source impedance is 600 Ω. If the length of the line is 10λ, determine antenna impedance.

3. Describe how matching is achieved using single stub matching. What are the advantages and disadvantages compared to double-stub matching?

4. Explain with sketches how the input impedance varies with frequency?

ASSIGNMENT QUESTIONS

1.Define the reflection coefficient & derive the expression for the input impedance in terms of reflection coefficient?

2. Explain and sketch the nature of variations of attenuation with frequency in a parallel plate wave guide for TE, TM and TEM waves?

13.4.8.1 OBJECTIVE QUESTIONS

1.Stub matching eliminates standing waves on
a) load side b) transmitter side c) both sides of stub d) none
8. Electromagnetic waves are reflected back by ionosphere due to their interaction with
a) Electrons d) Protons c) Ultra-violet rays d) Neutrons
2.A matching stub should be
a) nearest to load b) nearest to transmission end
c) mid-way between both d) anywhere between two
3.Impedance matching over wide frequency range can be obtained by using
a) double stubs b) single stubs c) quarter wave transformer d) none
4. The velocity of EM waves in free-space with respect to that in an RF cable with air dielectric is
a) increased b) decreased c) unchanged d) none
5.3 A (75 + j 50) load is connected to a coaxial transmission line of Z_O = 75 ohms at 10 GHz, the best method of matching consists in connecting
a) a short-circuited stub at the load
b) an inductance at the load
c) a capacitance at some specific distance from the load
d) a short-circuited stub at some specific distance from the load
6.To couple a coaxial line to a parallel wire line, it is best to use a
a) slotted line b) balun
c) directional coupler d) quarter wave transformer

7. In rectangular waveguides
a) $v_g v_p = c2$ b) $v_g v_p = 1$ c) $v_g v_p = 2c2$ d $v_g v_p$
8. A microstrip transmission line is
a) a thin metal strip placed within a waveguide
b) a thin metal strip placed within a circular coaxial line
c) a thin metal strip placed on a dielectric with a ground plane
d) a transmission line consisting of two parallel thin metal strips
9.Waveguide impedance Z_o of a rectangular waveguide for TE10 mode is
a) directly proportional to the width of the guide
b) inversely proportional to the width of the guide
c) does not depend on the width of the guide
d) directly proportional to double the width of the guide
10.Z_o of a parallel wire transmission line_____ with increase in distance between the conductors.
a) Increases b) decreases
c) does not change d) none of these
11. The characteristic impedance Z_o equals
a) Z_{OC} / Z_{SC} b) Z_{SC} / Z_{OC} c) $(Z_{SC} / Z_{OC})\ \lambda$ d) $(Z_{SC}.Z_{OC})\ \lambda$
12. A Smith chart is used for solving
a) propagation problems b) transmission problem
c) Antenna problems d) attenuation problems

13.To specify a mode in rectangular a rectangular waveguide, its electric field has to be defined in
a) one axis b) two axes c) three axes d) four axes
14.If a loss less line of 50 ohms terminated in a load Z_l has VSWR = 2.0 and the voltage maxima occurs with the load, the Zl is
a) 25 ohms b) 50 ohms c) 100 ohms d) 150 ohms
A lossless line will be distortion less if the phase shift constant
a) is constant with frequency
b) varies directly with frequency
c) varies inversely with frequency
d) has nothing to do with distortion on a lossless line.
Mark the wrong statements in the following:
15.The VSWR of a transmission line is infinity, the line is terminated in
a) a complex impedance b) open line c) a pure reactance d) short line
16.When an ideal transmission line is terminated in its character impedance, the first minimum is formed at the load end.
17.Transmission lines can be used for impedance matching?
18.Loading of cables reduces transmission loss?
19.Propagation in waveguides is below the critical frequency and independent of waveguide dimensions?
20. The input impedance of an infinite transmission line is equal to Characteristic impedance Z_O.

7.4.8.3. TUTORIAL TOPICS

1. Numerical on ¼, ½, 1/8 lines, Reflective coefficient, VSWR

8.ELECTRICAL ENGINEERING LAB

8.1 JNTUH SYLLABAUS

PART-A

1.Verification of KVL and KCL.
2. Serial and Parallel Resonance-Timing,Resonant frequency,bandwidth and Q-factor determine for RLC network
3.Time response of first order RC/RL network for periodic non- sinusoidal inputs-time constant and steady state error determine
4.Two port network parameters-Z-Y Parameters ,chain matrix and analytical verification
5.Verification of super position and reciprocity
6.Verification of maximum power transfer theorem.Verification on DC and AC excitation with Resistive and Reactive loads
7.Experimental determination of Thevenin's and Norton's equivalent circuits and verification by direct test.
8.Constant –k Low pass Filter and High pass Filter –Design and Test.

PART-B

1.Magnetization characteristics of DC shunt generator .Detrmination of crictical field Resistance.
2.Swinburne's Test on DC shunt machine (predetermination of efficiency of a given DC shunt machine working as motor and generator)
3.Brake test on DC shunt motor .Determination performance characteristics.
4.OC & SC test on single-phase transformer
5.Load Test on single Transformer

Note : Any 12 of the above experiments are to be conducted.

8.2.LAB SCHEDULE

Subject: Electrical Engineering Lab

S.No	Topic	Date Planned	Date Conducted
1			
2			
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9. ELECTRONIC CIRCUIT ANALYSIS LAB

9.1. JNTUH SYLLABUS

MINIMUM 12 EXPERIMENTS SHOULD BE CONDUCTED:

i)Design and Simulation in simulation Laboratory using any Simulation Software.
(Any 6 Experimets)

1.Common Emitter Amplifier
2.Common Source Amplifier
3.Two stage RC Coupled Amplifier
4.Current shunt and Voltage series Feed back amplifier
5.Cascode Amplifier
6.Wien bridge oscillator using transistor
7.RC Phasr shift oscillator using Tansistors
8.Class A Power amplifier
9.Class B complementary symmentry Amplifier
10.Common base(BJT)/Common gate(JFET) Amplifier

ii)Testing in the hardware Laboratory(6 Experiments)

A)Any three circuits simulated in Simulation laboratory
B)Any Three of the following
1. Class A Power Amplifier
2.Class C Power Amplifier
3.Single Tuned Voltage Amplifier
4.Hartley & Colpitt's Oscillators
5.Darlington pairs
6.MOS Amplifier

9.2.LAB SCHEDULE

Subject: Electronic Circuit Analysis LAB

S.No	Topic	Date Planned	Date Conducted
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10. PULSE AND DIGITAL CIRCUITS LAB

10.1.SYLLABUS

MINIMUM 12 EXPERIMENTS SHOULD BE CONDUCTED:

1. Linear Wave Shaping
2. Non- Linear Wave Shaping –clippers.
3. Non- Linear Wave Shaping –Clampers.
4. Transistor as a Switch.
5. Study of Logic Gates & Some applications.
6. Study of filp-flops & some applications.
7. Sampling Gates.
8. Astable Multivibrator.
9. Monostable Multivibrator.
10. Bistable Multivibrator.
11. Schmitt Trigger.
12 UJT Relaxation Oscillator.
13 Bootstrap Sweep Circuit.

10.2.LAB SCHEDULE

Subject: Pulse and Digital Circuits Lab

S.No	Topic	Date Planned	Date Conducted
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PLACEMENT CELL

MLR Institutions has a fulltime training and placement cell interacting with the Industry for Student and Faculty Development Programmes.

MLR Thas the unique distinction of placing their First Batch of B.Tech/MCA Students in their prefinal year Study and MBA Students in Multi National Companies like Satyam Computer Services Ltd., L&T Infotech Ltd, Infotech Enterprises Ltd, Dell International, Medha Servodrives Ltd, CyberNet Slash Support, GenPact, India Infoline, NoKia Ltd, ICICI Bank, Axis Bank, NCL Industries Ltd, 24x7 Customer, nLeague, Auro power Systems, Amazon.com, Exensys, Tesco.

The Institute has placed more than 100 Students in Placements/Internship Programmes and interacted with more than 60 Multi National Companies for Placements.

WIPRO, Airtel, Indiabulls, INFOMEDIA, VLS, Satyam, Husys, kotak Securities, GENPACT, India Infoline, ICICI Securities, India Infoline, BAJAJ CAPITAL, Mahindra Finance, MEDHA, AXIS BANK, Infotech, HDFC BANK We understand your world, MAX Your Partner for Life, AMEYA GROUP, RELIANCE Money, ValueLabs, CSS Cybernet - SlashSupport, L&T Infotech, Capital IQ A Division of Standard & Poor's, NOKIA, 24/7 Customer, TESCO, DELL, amazon.com, eXensys

Alumni Association:

MLR Institute of Technology conducted the First Alumni Meet of the Institute under the Chairmanship of Sri M Laxman Reddy with the First Outgoing MBA 2006-08 Batch on 14th February 2009. The Meet was to take feedback from Alumni Students to strengthen the bond between the Institute and alma matter and help the students to make a career and find a dream job in the industry of their own choice and help the Institute in filling the gap between Academia and Industry.

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GANDIMAISAMMA - MLRIT 3 KM