LABORATORY MANUAL
ELECTRONIC CIRCUITS LAB

II B.TECH -II SEMESTER (EEE)

AY-2018-2019

Prepared by
Lab In-charge:

T.IMMANUEL
S SINDHU REKHA

CERTIFICATE

This is to certify that this manual is a bonafide record of practical work in the ***Electronics*** **Circuits** ***Laboratory*** in **Second Semester of II-year B. Tech (EEE) programme** during the academic year **2018-19**. This book is prepared by **Mr.T.Immanuel, (Asst. Professor), Mrs. S. SindhuRekha (Asst. Professor),**Department of Electronics and Communication Engineering.

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PREFACE

This laboratory lays the foundation for the Electronics and Communication Engineering students during second year of their course.

Circuits and components of EC Lab can be divided into 2 groups: Analog And Digital. In Hardware lab, the students design, construct and test the working of analog circuits such as transistor amplifiers, operational amplifiers and oscillators.. After performing all the experiments included in this Laboratory, it is hoped the student receives good training to handle any electronic equipment available in electronics field.

Basic electronic equipment used in electronics laboratory

- Cathode Ray Oscilloscope to view and measure AC waveforms.
- Function Generator used to design, develop and to trouble shoot electronic equipments
- Regulated power supply to supply DC voltage to electronic circuits.
- Breadboard to mount the components temporarily for experimental work.
- IC Trainer kits to design sequential and combinational logic circuits

By,

T.IMMANUEL,
S. SINDHUREKHA

ACKNOWLEDGEMENT

It was really a good experience, working with ***Electronics circuits*** lab. First we would like to thank Mr.K.Naga Bhushanam, Assoc.Professor, HOD of Department of Electronics and Communication Engineering, Marri Laxman Reddy Institute of technology & Management for his concern and giving the technical support in preparing the document.

We are deeply indebted and gratefully acknowledge the constant support and valuable patronage of Dr.R.Kotaih, Director, Marri Laxman Reddy Institute of technology & Management for giving us this wonderful opportunity for preparing the ***Electronics circuits*** laboratory manual.

We express our hearty thanks to Dr.K.Venkateswara Reddy, Principal, Marri Laxman Reddy Institute of technology & Management, for timely corrections and scholarly guidance.

At last, but not the least I would like to thanks the entire ECE Department faculty those who had inspired and helped us to achieve our goal.

By,

T.IMMANUEL,
S. SINDHUREKHA

GENERAL INSTRUCTIONS

1. Students are instructed to come to ***Electronic Devices and Circuits*** laboratory on time. Late comers are not entertained in the lab.

2. Students should be punctual to the lab. If not, the conducted experiments will not be repeated.

3. Students are expected to come prepared at home with the experiments which are going to be performed.

4. Students are instructed to display their identity cards before entering into the lab.

5. Students are instructed not to bring mobile phones to the lab.

6. Any damage/loss of equipments like transformers, transistors, CRO's etc., during the lab session, it is student's responsibility and penalty or fine will be collected from the student.

7. Students should update the records and lab observation books session wise. Before leaving the lab the student should get his lab observation book signed by the faculty.

8. Students should submit the lab records by the next lab to the concerned faculty members in the staffroom for their correction and return.

9. Students should not move around the lab during the lab session.

10. If any emergency arises, the student should take the permission from faculty member concerned in written format.

11. The faculty members may suspend any student from the lab session on disciplinary grounds.

12. Never copy the output from other students. Write down your own outputs.

INSTITUTION VISION AND MISSION

VISION

To be as an ideal academic institution by graduating talented engineers to be ethically strong, competent with quality research and technologies

MISSION

To fulfill the promised vision through the following strategic characteristics and aspirations:

- Utilize rigorous educational experiences to produce talented engineers
- Create an atmosphere that facilitates the success of students
- Programs that integrate global awareness, communication skills and Leadership qualities
- Education and Research partnership with institutions and industries to prepare the students for interdisciplinary research

DEPARTMENT VISION, MISSION, PROGRAMME EDUCATIONAL OBJECTIVES AND SPECIFIC OUTCOMES

Vision and Mission

Our Vision

Imparting quality technical education through research, innovation and team work for a lasting technology development in the area of Electronics and Communication Engineering.

Our Mission

To develop a strong centre of excellence for education and research with excellent infrastructure and well qualified faculties to instill in them a passion for knowledge.

To achieve the Mission the department will

1. Establish a unique learning environment to enable the students to face the challenges of the Electronics and Communication Engineering field.
2. Promote the establishment of centre of excellence in niche technology areas to nurture the spirit of innovation and creativity among faculty and students.
3. Provide ethical and value based education by promoting activities addressing the societal needs.
4. Enable students to develop skills to solve complex technological problems of current times and also provide a framework for promoting collaborative and multidisciplinary activities.

PEO's & PO's

PROGRAMME EDUCATIONAL OBJECTIVES

PEO 1: Have successful **careers in Industry.**

PEO 2: Show excellence in **higher studies/ Research.**

PEO 3: Show good competency towards **Entrepreneurship.**

PROGRAM OUTCOMES

a An ability to apply knowledge of Science, Mathematics, Engineering & Computing fundamentals for the solutions of Complex Engineering problems

b An ability to identify, formulates, research literature and analyze complex engineering problems using first principles of mathematics and engineering sciences.

c An ability to design solutions to complex process or program to meet desired needs.

d Ability to use research-based knowledge and research methods including design of experiments to provide valid conclusions.

e An ability to use appropriate techniques, skills and tools necessary for computing practice.

f Ability to apply reasoning informed by the contextual knowledge to assess social issues, consequences & responsibilities relevant to the professional engineering practice.

g Ability to understand the impact of engineering solutions in a global, economic, environmental,

and societal context with sustainability.

h An understanding of professional, ethical, Social issues and responsibilities.

i An ability to function as an individual, and as a member or leader in diverse teams and in multidisciplinary settings.

j An ability to communicate effectively on complex engineering activities within the engineering community.

k Ability to demonstrate and understanding of the engineering and management principles as a member and leader in a team.

l Ability to engage in independent and lifelong learning in the context of technological change.

PROGRAM SPECIFIC OUTCOMES

PSO1 Analyze and design analog & digital circuits or systems for a given specification and function.

PSO2 Implement functional blocks of hardware-software co-designs for signal processing and communication applications.

COURSE STRUCTURE, OBJECTIVES & OUTCOMES

Laboratory subjects – Internal and external evaluation– Details of marks

Electronics Circuits lab will have a continuous evaluation during 4thsemester for 25 sessional marks and 75 end semester examination marks.

Out of the 25 marks for internal evaluation, day-to-day work in the laboratory shall be evaluated for 15 marks and internal practical examination shall be evaluated for 10 marks conducted by the laboratory teacher concerned.

The end examination will be evaluated for a maximum of 75 marks.The end semester examination shall be conducted with an external examiner and internal examiner. The external examiner shall be appointed by the principal / Chief Controller of examinations

Course Objectives:

The objective of this lab is to make the students

- To understand the basic working principle of electronic devices.
- To specify various active and passive electronic components and devices and identify the terminals and to draw the symbols for different electronic components.
- To understand and operate multimeter for current, voltage and resistance measurements.
- To design electronic circuits for various applications using multisim software .
- To investigate / test / verify property or characteristics of electronic devices, amplifiers and oscillators
- To implement and verify logic gates, sequential and combinational logic circuits.
- To learn operating principle and applications of electronic circuits and devices like amplifier, oscillator.

LIST OF EXPERIMENTS:

EE408ES: ELECTRONIC CIRCUITS LAB

B.Tech. II Year II Sem. L T P C
0 0 3 2

Prerequisite: Electronic Circuits& Switching theory and Logic Design

Course Objectives:
- To design and simulate various BJT and FET Voltage and Power amplifiers.
- To design and simulate various BJT Feedback amplifiers.
- To design and simulate various BJT Oscillators.
- To design and simulate linear and non linear wave shaping circuits

Course Outcomes: After completion of this lab the student is able to
- Apply the concepts of amplifiers in the design of Public Addressing System
- Generate Sinusoidal wave forms
- Design stable system using feedback concepts.
- Design multi vibrator using transistor

The following experiments are required to be conducted compulsory experiments:

1. CE amplifier.

2. CC amplifier (Emitter Follower).

3. FET amplifier (Common Source).

4. Wien bridge and RC Phase shift Oscillator.

5. Current series and Voltage series Feedback Amplifier.

6. Colpitt and Hartley Oscillator.

7. Double stage RC coupled amplifier.

8. Clippers and Clampers

In addition to the above eight experiments, at least any two of the experiments from the Following list are required to be conducted:

9. Transistor as a switch

10. Study of Logic gates & some applications

11. Study of Flip-Flops and some applications.

12. Mono-stable &A stable multi-vibrators.

13. Bi-stable multi-vibrator & Schmitt trigger**.**

EXPT NO: 1

COMMON EMITTER AMPLIFIER

AIM: -

1. Plot the frequency response of a BJT amplifier in common emitter configuration.
2. Calculate gain.
3. Calculate bandwidth.

COMPONENTS & EQUIPMENTS REQUIRED: -

S.No	Device	Range/Rating	Qty
1.	(a) DC supply voltage (b) BJT (c) Capacitors (d) Resistors	12V BC107 BP 100 F,10 F 5.6K ,10k ,22K ,,1k 220 ,	1 1 2,1 Each 1NO
2.	Signal generator	0.1Hz-1MHz	1
3.	CRO	0Hz-20MHz	1
4.	Connecting wires	5A	4

CIRCUIT DIAGRAM:

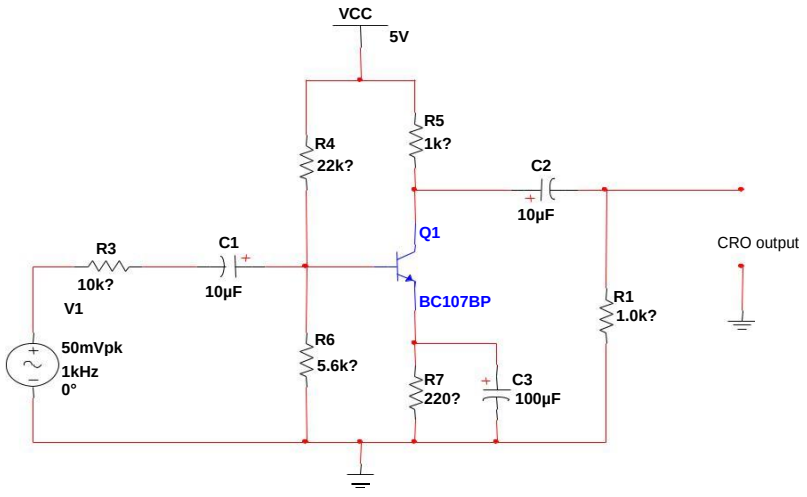


Fig: 1. Common Emitter Amplifier circuit diagram

PROCEDURE: -

1. Connect the circuit diagram as shown in figure for common emitter amplifier.
2. Adjust input signal amplitude in the function generator and observe an amplified voltage at the output without distortion.
3. By keeping input signal voltage, say at 50mV, vary the input signal frequency from 0 to 1MHz in steps as shown in tabular column and note the corresponding output voltages.
4. Find the voltage gain, $A_V = \frac{V_O}{V_{in}}$, $A_{V(dB)} = 20\log \frac{V_O}{V_{in}}$
5. Plot A_V Vs frequency on a semi-log sheet.

PRECAUTIONS:

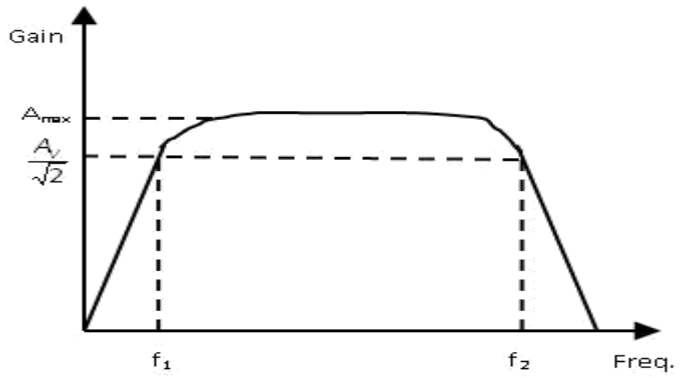
Avoid loose connections give proper input voltage

TABULAR COLUMN: **Input = 50mV**

Frequency(in Hz)	OutputVoltage (V_o)	Gain $A_v=V_o/V_i$	Gain(in dB) $=20\log_{10}(V_o/V_i)$
20			
50			
100			
1k			
10k			
100k			
200,500K			
1M			

RESULT: -

1. Frequency response of BJT amplifier is plotted.
2. Gain = _____dB (maximum).
3. Bandwidth= f_H--f_L = _____Hz.



APPLICATIONS:

1. The common emitter circuit is popular because it's well-suited for voltage amplification, especially at low frequencies.
2. Common-emitter amplifiers are also used in radio frequency transceiver circuits.
3. Common emitter configuration commonly used in low-noise amplifiers.

VIVA QUESTIONS:

1. Why the CE amplifier provides a phase reversal?
2. In the dc equivalent circuit of an amplifier, how are capacitors treated?
3. What is the effect of bypass capacitor on frequency response?
4. Define lower and upper cutoff frequencies for an amplifier.
5. State the reason for fall in gain at low and high frequencies.
6. What is meant by unity gain frequency?
7. Define Bel and Decibel.
8. What do we represent gain in decibels?
9. Why do you plot the frequency response curve on a semi-log paper?
10. Explain the function of emitter bypass capacitor C_E?
11. What is the equation for voltage gain?
12. What is cut off frequency? What is lower 3dB and upper 3dB cut off frequency?
13. What are the applications of CE amplifier?
14. What is active region?
15. What is Bandwidth of an amplifier?
16. What is the importance of gain bandwidth product?
17. Draw h parameter equivalent circuit of CE amplifier.
18. What is the importance of coupling capacitors in CE amplifier?
19. What is the importance of emitter by pass capacitor?
20. What type of feedback is used in CE amplifier?
21. What are the various types of biasing a Transistor?
22. What is Q point of operation of the transistor? What is the region of operation of the transistor when it is working as an amplifier?
23. Why frequency response of the amplifier is drawn on semi-log scale graph?
24. If Q point is not properly selected, then what will be the effect on the output waveform?
25. What are the typical values of the input impedance and output impendence of CE amplifier?
26. What is meant by unity gain frequency?
27. Define Bel and Decibel?
28. What do we represent gain in decibels?
29. Why do you plot the frequency response curve on a semi-log paper?
30. In the dc equivalent circuit of an amplifier, how are capacitors treated?

EXERCISE:

1. Input & output characteristics of BC 107 transistor in CE configuration with R_I = 50K.
2. Input & output characteristics of BC 107 transistor in CE configuration with R_O = 2K.
3. I/O characteristics of BC 107 transistor in CE configuration with R_I = 50K R_O = 2K
4. Input & output characteristics of BC 107 transistor in CE configuration with R_I = 150K.
5. I/O characteristics of BC 107 transistor in CE configuration with R_I = 150K R_O = 2K
6. Input & output characteristics of SL 100 transistor in CE configuration with R_I = 50K.
7. Input & output characteristics of SL 100 transistor in CE configuration with R_O = 2K.
8. I/O characteristics of PNP transistor in CE configuration with R_I = 50K R_O = 2K
9. Input & output characteristics of PNP transistor in CE configuration with R_I = 150K.
10. I/O characteristics of PNP transistor in CE configuration with R_I = 150K R_O = 2K
11. Input & output characteristics of BC 107 transistor in CE configuration with R_I = 50K.
12. Input & output characteristics of BC 107 transistor in CE configuration with R_O = 2K.
13. I/O characteristics of BC 107 transistor in CE configuration with R_I = 50K R_O = 2K
14. Input & output characteristics of BC 107 transistor in CE configuration with R_I = 150K.
15. I/O characteristics of BC 107 transistor in CE configuration with R_I = 150K R_O = 2K
16. Input & output characteristics of SL 100 transistor in CE configuration with R_I = 50K.
17. Input & output characteristics of SL 100 transistor in CE configuration with R_O = 2K.
18. I/O characteristics of PNP transistor in CE configuration with R_I = 50K R_O = 2K
19. Input & output characteristics of PNP transistor in CE configuration with R_I = 150K.
20. I/O characteristics of PNP transistor in CE configuration with R_I = 150K R_O = 2K
21. Input & output characteristics of BC 107 transistor in CE configuration with R_I = 50K.
22. Input & output characteristics of BC 107 transistor in CE configuration with R_O = 2K.
23. I/O characteristics of BC 107 transistor in CE configuration with R_I = 50K R_O = 2K
24. Input & output characteristics of BC 107 transistor in CE configuration with R_I = 150K.
25. I/O characteristics of BC 107 transistor in CE configuration with R_I = 150K R_O = 2K
26. Input & output characteristics of SL 100 transistor in CE configuration with R_I = 50K.
27. Input & output characteristics of SL 100 transistor in CE configuration with R_O = 2K.
28. I/O characteristics of PNP transistor in CE configuration with R_I = 50K R_O = 2K
29. Input & output characteristics of PNP transistor in CE configuration with R_I = 150K.
30. I/O characteristics of PNP transistor in CE configuration with R_I = 150K R_O = 2K

EXPT NO: 2

COMMON COLLECTOR AMPLIFIER (EMITTER FOLLOWER)

AIM: -

1. To plot frequency response of CC amplifier and calculate gain & bandwidth.

EQUIPMENTS & COMPONENTS REQUIRED:

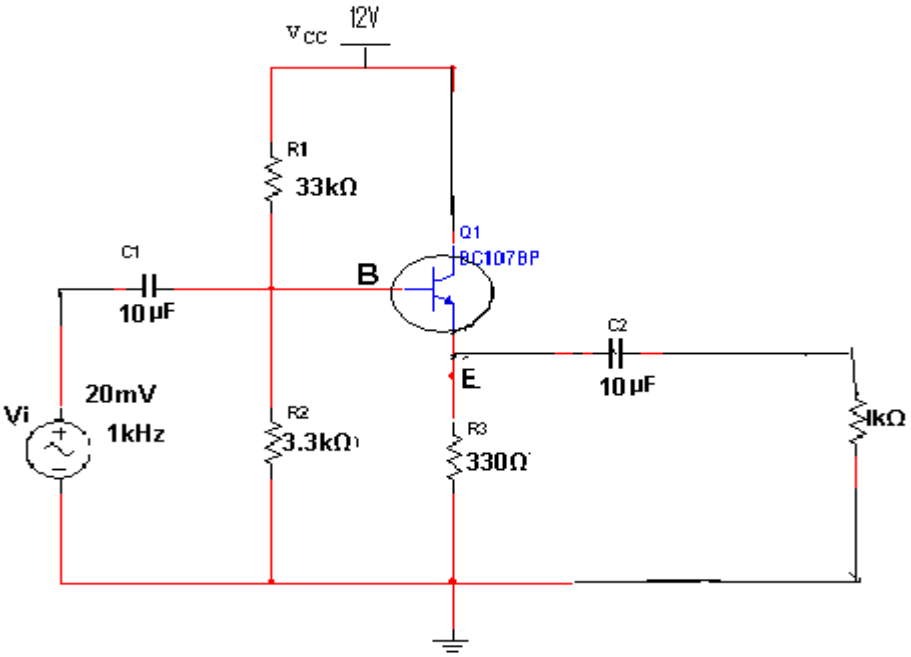
S.No	Device	Range/Rating	Qty
1.	(a) Regulated DC supply voltage	0-30V	1
2	Function generator	1MHz	1
2.	Dual trace CRO(oscilloscope)	25MHz	1
3.	BJT	BC107 OR 2N2222,BC547	1
4.	Connecting wires		
5.	Capacitor	10µf=2,100 µf	
6.	Resistor		

THEORY:

A transistor is a three terminal active device. The terminals are emitter, base, collector. In CB configuration, the base is common to both input (emitter) and output (collector). For normal operation, the E-B junction is forward biased and C-B junction is reverse biased. In CB configuration, IE is +ve, IC is –ve and IB is –ve. So, VEB=f1 (VCB,IE) and IC=f2 (VCB,IB) With an increasing the reverse collector voltage, the space-charge width at the output junction increases and the effective base width 'W' decreases. This phenomenon is known as "Early effect". Then, there will be less chance for recombination within the base region. With increase of charge gradient within the base region, the current of minority carriers injected across the emitter junction increases.The current amplification factor of CB configuration is given by, $\alpha = \Delta IC / \Delta IE$

In common-collector amplifier the input is given at the base and the output is taken at the emitter. In this amplifier, there is no phase inversion between input and output. The input impedance of the CC amplifier is very high and output impedance is low. The voltage gain is less than unity. Here the collector is at ac ground and the capacitors used must have a negligible reactance at the frequency of operation. This amplifier is used for impedance matching and as a buffer amplifier. This circuit is also known as emitter follower.

CIRCUIT DIAGRAM:



PROCEDURE: -

1. Connect the circuit according to the circuit diagram as shown in figure on breadboard.

2. Set the power supply at 12V and function generator signal amplitude (20 to 50mV) for (sine wave) 1 KHz frequency on CH-1knob to minimum position.

3. FEED the signal sine wave (20 to 50mV) to the input of CE amplifier and observe the Vi voltage on Ch-1 &output Vo voltage on Ch-2..

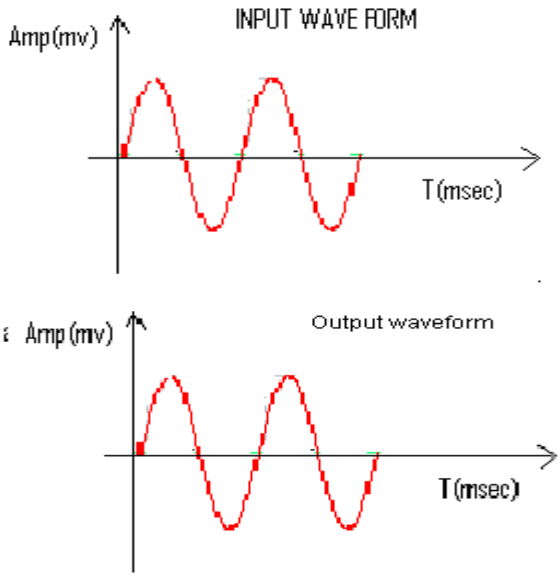
4. keeping the input signal unchanged select the range switch (10Hz-1MHz) in steps.

5. Note down the Vo output voltage amplitude for different frequency {15H, 25Hz, 100Hz…1MHz}

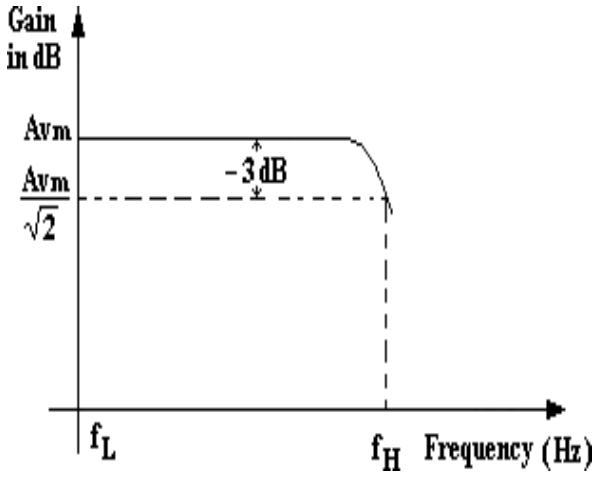
6. Tabulate the results in tabular form.

7. After calculation Av and gain in dB using semi-logarithm sheet plot the curve.

WAVEFORM:



Frequency Response Curve



PRECAUTIONS:

1. The input voltage must be kept constant while taking frequency response.
2. Proper biasing voltages should be applied.

RESULT:

The voltage gain and frequency response of the CC amplifier are obtained. Also gain Bandwidth product is calculated.

REALTIME APPLICATIONS:

The low output impedance allows a source with a large output impedance to drive a small load impedance; it functions as a voltage buffer. In other words, the circuit has current gain (which depends largely on the h_{FE} of the transistor) instead of voltage gain. A small change to the input current results in much larger change in the output current supplied to the output load.
One aspect of buffer action is transformation of impedances. For example, the Thévenin resistance of a combination of a voltage follower driven by a voltage source with high Thévenin resistance is reduced to only the output resistance of the voltage follower (a small resistance). That resistance reduction makes the combination a more ideal voltage source. Conversely, a voltage follower inserted between a small load resistance and a driving stage presents a large load to the driving stage—an advantage in coupling a voltage signal to a small load.
This configuration is commonly used in the output stages of class-B and class-AB amplifiers. The base circuit is modified to operate the transistor in class-B or AB mode. In class-A mode, sometimes an active current source is used instead of R_E(Fig. 4) to improve linearity and/or efficiency.[1]

VIVA QUESTIONS:

1. What are the applications of CC amplifier?
2. What is the voltage gain of CC amplifier?
3. What are the values of input and output impedances of the CC amplifier?
4. To which ground the collector terminal is connected in the circuit?
5. Identify the type of biasing used in the circuit?
6. Give the relation between α, β and γ.
7. Write the other name of CC amplifier?
8. What are the differences between CE, CB and CC?
9. When compared to CE, CC is not used for amplification. Justify your answer?
10. What is the phase relationship between input and output in CC?
11. What is the type of capacitor used in RC coupled amplifier for a) coupling two phases
12. What is signal source used for experiment of an RC coupled amplifier and how much maximum voltage it could give
13. How do you determine AC power output in class A amplifier i.e., do you measure current or voltage and how?
14. What are the applications of CC amplifier?
15. What is the voltage gain of CC amplifier?
16. What are the values of input and output impedances of the CC amplifier?
17. To which ground the collector terminal is connected in the circuit?
18. Identify the type of biasing used in the circuit?
19. Give the relation between α, β and γ.
20. Write the other name of CC amplifier?
21. What are the differences between CE, CB and CC?
22. When compared to CE, CC is not used for amplification. Justify your answer?
23. What is the phase relationship between input and output in CC?
24. Give the relation between α, β and γ.
25. Write the other name of CC amplifier?
26. What are the differences between CE, CB and CC?
27. When compared to CE, CC is not used for amplification. Justify your answer?
28. What is the phase relationship between input and output in CC?

29. What is the type of capacitor used in RC coupled amplifier for a) coupling two phases b) by pass emitter
30. Give the relation between α, β and γ?

Design Problems

1. Plot the frequency response of CC amplifier with R_S = 100 Ω using BC 107?

2. Plot the frequency response of CC amplifier with R_E = 240 Ω using BC 107?

3. Plot the frequency response of CC amplifier with R_{B1} = 10 KΩ using BC 107?

4. Plot the frequency response of CC amplifier with R_{B2} = 60 KΩ using BC 107?

5. Plot frequency response of CC amplifier triangular I/P with R_S = 100 Ω using BC 107?

6. Plot the frequency response of CC amplifier with R_E = 240 Ω using PNP Transistor?

7. Plot the frequency response of CC amplifier with R_{B2} = 60 KΩ using PNP Transistor?

8. Plot the frequency response of CC amplifier with R_{B1} = 10 KΩ using SL 100?

9. Plot frequency response of CC amplifier triangular I/P with R_S = 100 Ω using PNP?

10. Plot frequency response of CC amplifier Square I/P with R_S = 100 Ω using BC 107?

11. Plot the frequency response of CC amplifier with R_S = 500 Ω using BC 107?

12. Plot the frequency response of CC amplifier with R_E = 940 Ω using BC 107?

13. Plot the frequency response of CC amplifier with R_{B1} = 50 KΩ using BC 107?

14. Plot the frequency response of CC amplifier with R_{B2} = 66 KΩ using BC 107?

15. Plot frequency response of CC amplifier triangular I/P with R_S = 500 Ω using BC 107?

16. Plot the frequency response of CC amplifier with R_E = 940 Ω using PNP Transistor?

17. Plot the frequency response of CC amplifier with R_{B2} = 66 KΩ using PNP Transistor?

18. Plot the frequency response of CC amplifier with R_{B1} = 50 KΩ using SL 100?

19. Plot frequency response of CC amplifier triangular I/P with R_S = 500 Ω using PNP?

20. Plot frequency response of CC amplifier Square I/P with R_S = 500 Ω using BC 107

EXPT NO: 3

FET (COMMON SOURCE AMPLIFIER)

AIM: -

1. Plot the frequency response of a FET amplifier in common source mode.
2. Calculate gain.
3. Calculate bandwidth.

COMPONENTS & EQUIPMENTS REQUIRED: -

S.No	Device	Range/Rating	QTY
1.	(a) DC supply voltage	12V	1
	(b) FET	BFW	1
	(c) Capacitors	11,BF245C	2
		10 F	1
	(d) Resistors	100 F	1
		100 ,470	1
		4.7K ,8.2k	
2.	Signal generator	0.1Hz-1MHz	1
3.	CRO	0Hz-20MHz	1
4.	Connecting wires	5A	4

CIRCUIT DIAGRAM:

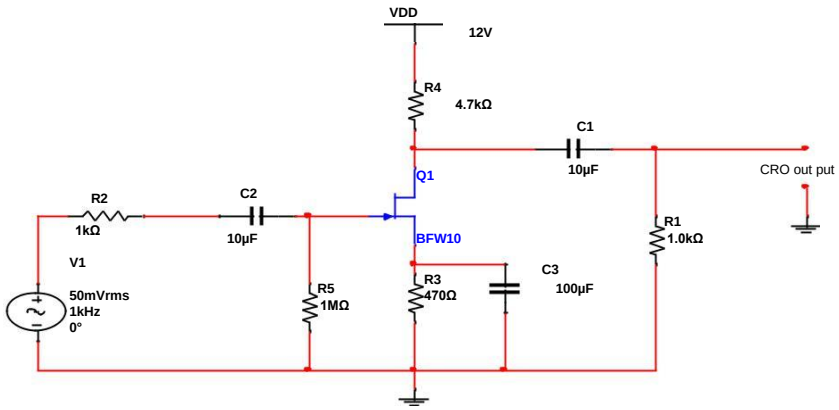


Fig: 3. Common Source Amplifier circuit

PROCEDURE: -

1. Connect the circuit diagram as shown in figure.
2. Adjust input signal amplitude 50mV, 1 KHz in the function generator and Observe an amplified voltage at the output without distortion.
3. By keeping input signal voltage, say at 50mV; vary the input signal frequency from 10 to 1MHz in steps as shown in tabular column and note the corresponding output voltages.

PRECAUTIONS:

1. Avoid loose connections and give proper input Voltage

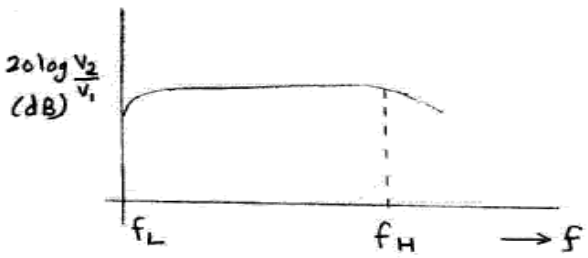
TABULAR COLUMN: **Input = 50mV**

Frequency(in Hz)	Output Voltage (V_o)	Gain $A_v=V_o/V_i$	Gain(in dB) $=20\log_{10}(V_o/V_i)$
10			
50			
100			
1K			
10k			
50K,100K			
200k,500K			
1M			

RESULT: -

1. Frequency response of FET Common source amplifier is plotted.
2. Gain = _____dB (maximum).
3. Bandwidth= f_H--f_L = _____Hz.

EXPECTED GRAPH:



REALTIME APPLICATIONS:

The common-source (CS) amplifier may be viewed as a transconductance amplifier or as a voltage amplifier. (See classification of amplifiers). As a transconductance amplifier, the input voltage is seen as modulating the current going to the load. As a voltage amplifier, input voltage modulates the amount of current flowing through the FET, changing the voltage across the output resistance according to Ohm's law. However, the FET device's output resistance typically is not high enough for a reasonable transconductance amplifier (ideally infinite), nor low enough for a decent voltage amplifier (ideally zero). Another major drawback is the amplifier's limited high-frequency response. Therefore, in practice the output often is routed through either a voltage follower (common-drain or CD stage), or a current follower (common-gate or CG stage), to obtain more favorable output and frequency characteristics. The CS–CG combination is called a cascode amplifier

VIVA QUESTIONS:

1. What is Miller effect on common source amplifier?
2. What is the purpose of source resistor and gate resistor?
3. What is swamping resistor
4. What is the purpose of swamping resistor in common source amplifier
5. FET is a liner or non-linear device. And justify your answer
6. What is square law and give an example for a square law device Why FET is called as uni-polar device?
7. Why the common-source (CS) amplifier may be viewed as a trans-conductance amplifier or as a voltage amplifier?
8. What are the characteristics of JFET source amplifier?
9. What is the impedance of FET?
10. What are the comparisons and differences between a BJT and a JFET?
11. What is meant by a uni-polar device?
12. Why is a JFET known as a uni-polar Device?
13. Draw the symbols of JFET, MOSFET?
14. What are the typical applications of a JFET?
15. Explain pinch off voltage and region?
16. What is Bandwidth of an amplifier?
17. What is the importance of gain bandwidth product?
18. What are the characteristics of JFET source amplifier? What is the impedance of FET?
19. What is an amplifier?
20. If a Q point is not properly selected, then what will be the effect on the output waveform?
21. What is the purpose of swamping resistor in common source amplifier
22. FET is a liner or non-linear device. And justify your answer
23. What is square law and give an example for a square law device Why FET is called as
24. Why FET is called as unipolar device?
25. Why the common-source (CS) amplifier may be viewed as a trans-conductance amplifier
26. What are the characteristics of JFET source amplifier?
27. What are the characteristics of JFET source amplifier?
28. What is the impedance of FET?
29. What is an amplifier?
30. If Q point is not properly selected, then what will be the effect on the output waveform?

EXERCISE:

1. Plot the frequency and amplitude response of FET BFW 10 amplifier with C_1 = 5 µF.
2. Plot the frequency response of FET BFW 10 amplifier with C_2 = 5 µF with triangular i/p.
3. Plot the amplitude response of FET BFW 10 amplifier with R_{G1} = 4.1 K.
4. Plot the amplitude response of FET BFW 10 amplifier with R_{G2} = 9.4 K triangular i/p.
5. Plot frequency response of BFW 10 amplifier R_{G1} = 4.1 K, R_{G2} = 9.4 K with square i/p.
6. Plot the frequency and amplitude response of FET BFW 11 amplifier with C_1 = 5 µF.
7. Plot the frequency response of P Channel JFET amplifier with C_2 = 5 µF, triangular i/p.
8. Plot the amplitude response of FET BFW 11 amplifier with R_{G1} = 4.1 K.
9. Plot the amplitude response of P Channel JFET amplifier with R_{G2} = 9.4 K triangular i/p.
10. Plot frequency response of P Channel JFET R_{G1} = 4.1 K, R_{G2} = 9.4 K with square i/p.
11. Plot the frequency and amplitude response of FET BFW 10 amplifier with C_1 = 10 µF.
12. Plot the frequency response of FET BFW 10 amplifier with C_2 = 2 µF with triangular i/p.
13. Plot the amplitude response of FET BFW 10 amplifier with R_{G1} = 2.1 K.
14. Plot the amplitude response of FET BFW 10 amplifier with R_{G2} = 5.4 K triangular i/p.
15. Plot frequency response of BFW 10 amplifier R_{G1} = 2.1 K, R_{G2} = 2.4 K with square i/p.
16. Plot the frequency and amplitude response of FET BFW 11 amplifier with C_1 = 2 µF.
17. Plot the frequency response of P Channel JFET amplifier with C_2 = 2 µF, triangular i/p.
18. Plot the amplitude response of FET BFW 11 amplifier with R_{G1} = 2.1 K.
19. Plot the amplitude response of P Channel JFET amplifier with R_{G2} = 2.4 K triangular i/p.
20. Plot frequency response of P Channel JFET R_{G1} = 2.1 K, R_{G2} = 9.4 K with square i/p.
21. Plot the frequency and amplitude response of FET BFW 10 amplifier with C_1 = 5 µF.
22. Plot the frequency response of FET BFW 10 amplifier with C_2 = 5 µF with triangular i/p.
23. Plot the amplitude response of FET BFW 10 amplifier with R_{G1} = 4.1 K.
24. Plot the amplitude response of FET BFW 10 amplifier with R_{G2} = 9.4 K triangular i/p.
25. Plot frequency response of BFW 10 amplifier R_{G1} = 4.1 K, R_{G2} = 9.4 K with square i/p.
26. Plot the frequency and amplitude response of FET BFW 11 amplifier with C_1 = 5 µF.
27. Plot the frequency response of P Channel JFET amplifier with C_2 = 5 µF, triangular i/p.
28. Plot the amplitude response of FET BFW 11 amplifier with R_{G1} = 4.1 K.
29. Plot the amplitude response of P Channel JFET amplifier with R_{G2} = 9.4 K triangular i/p.
30. Plot frequency response of P Channel JFET R_{G1} = 4.1 K, R_{G2} = 9.4 K with square i/p

EXPT NO: 4

WEIN BRIDGE OSCILLATOR

AIM: To study the frequency response of Oscillator, calculate voltage gain and bandwidth from the response.

COMPONENTS AND EQUIPMENTS REQUIRED:

S.No	Device	Range/ Rating	Qty
1	a) DC supply voltage	12V	1
	b) Capacitor	10 F	2
	c) Resistor	10K ,4.7K ,27K	3
		22K ,3.3K ,39K	3
		1K ,	1
	d) NPN Transistor	2N3904	2
2	CRO	(0-20) MHz	1
3.	BNC Connector		1
3	Connecting wires	5A	6

CIRCUIT DIAGRAM:

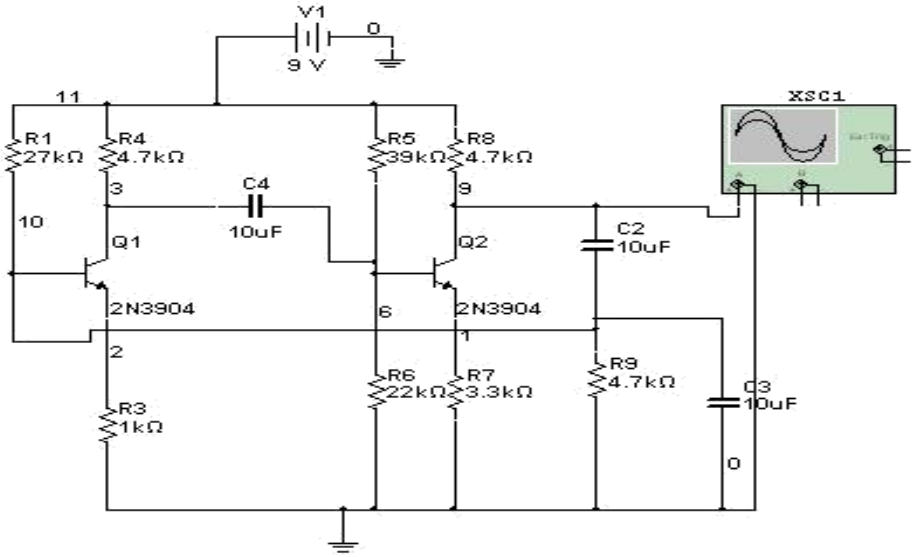


Fig: 4 Wien bridge oscillator circuit diagram

PROCEDURE:

1. Connect the circuit as shown in figure.
2. Connect the 0.0022 F capacitors in the circuit and observe the waveform.
3. Time period of the waveform is to be noted and frequency should be calculated by the formula f = 1/T.
4. Now fix the capacitance to 0.033 F and 0.01 F and calculate the frequency and tabulate as shown.
5. Find theoretical frequency from the formula f = 1/2 RC 6 and compare theoretical and practical frequencies.

OBSERVATIONS:

From CRO:

1. Amplitude of the output wave form
2. Time period of the signal

CALCULATIONS:

Theoretically:

Where R =

C =

$$f = \frac{1}{2x\ xRxC} =$$

RESULT: -

1. For C = 0.0022 F & R=10K
   Theoretical frequency=
   Practical frequency=
2. For C = 0.0033 F & R=10K
   Theoretical frequency=
   Practical frequency=
3. For C = 0.01 F & R=10K

Theoretical frequency=
Practical frequency=

APPLICATIONS:

1. It is used to measure the audio frequency.

2. Wien bridge oscillator designs the long range of frequencies
it produces sine wave

EXERCISE PROBLEMS:

1. Plot the Amplitude response of 2N3904 Oscillator with C_1 = 5 µF.
2. Plot the Amplitude response of 2N2222 Oscillator C2 = 5 µF with i/p.
3. Plot the Amplitude response of BC107 Oscillator with R_1 = 4.1 K.
4. Plot the Amplitude response of BC 547 Oscillator with R_2 = 9.4 K i/p.
5. Plot the Amplitude response of BC 548 Oscillator R1 = 4.1 K, R_2 = 9.4 K with i/p.
6. Plot the Amplitude response of BC 557 Oscillator with C_1 = 5 µF.
7. Plot the Amplitude response of BC 547 Oscillator with C_2 = 5 µF, i/p.
8. Plot the Amplitude response of 2N3904 Oscillator with R_1 = 4.1 K.
9. Plot the Amplitude response of 2N3904 Oscillator with R_2 = 9.4 K i/p.
10. Plot the Amplitude response of 2N3904 Oscillator R1 = 4.1 K, R_2 = 9.4 K with i/p.
11. Plot the Amplitude response of 2N3904 Oscillator with C_1 = 10 µF.
12. Plot the Amplitude response of CL100 Oscillator with C_2 = 2 µF with i/p.
13. Plot the Amplitude response of CL 100 Oscillator with R_1 = 2.1 K.
14. Plot the Amplitude response of CK 100 Oscillator with R_2 = 5.4 K i/p.
15. Plot the Amplitude response of 2N3904 Oscillator R1 = 2.1 K, R_2 = 2.4 K with i/p.
16. Plot the Amplitude response of 2N3904 Oscillator with C_1 = 2 µF.
17. Plot the Amplitude response of 2N3904 Oscillator with C_2 = 2 µF, i/p.
18. Plot the Amplitude response of 2N3904 Oscillator with R_1 = 2.1 K.
19. Plot the Amplitude response of SL100 Oscillator with R_2 = 2.4 K i/p.
20. Plot the Amplitude response of 2N3904 Oscillator R1 = 2.1 K, R_2 = 9.4 K with i/p.
21. Plot the Amplitude response of 2N3904 Oscillator with C_1 = 5 µF.
22. Plot the Amplitude response of 2N3904 Oscillator with C_2 = 5 µF with i/p.
23. Plot the Amplitude response of 2N3904 Oscillator with R_1 = 4.1 K.
24. Plot the Amplitude response of 2N3904 Oscillator with R_2 = 9.4 K i/p.
25. Plot the Amplitude response of 2N3904 Oscillator R1 = 4.1 K, R_2 = 9.4 K with i/p.
26. Plot the Amplitude response of 2N3904 Oscillator with C_1 = 5 µF.
27. Plot the Amplitude response of 2N3904 Oscillator C2 = 5 µF, i/p.
28. Plot the Amplitude response of 2N3904 Oscillator with R_1 = 4.1 K.
29. Plot the Amplitude response of 2N3904 Oscillator with R_2 = 9.4 K i/p.
30. Plot the Amplitude response of 2N3904 Oscillator of R_1 = 4.1 K, R_2 = 9.4 K with i/p

VIVA QUESTIONS:

1. Mention two essential conditions for a circuit to maintain oscillations?
2. What is the major disadvantage of a Twin-T oscillator?
3. Differentiate oscillator from amplifier?
4. State Barkhausen criterion for sustained oscillation. What will happen to the oscillation if the magnitude of the loop gain is greater than unity?
5. Why an LC tank circuit does not produce sustained oscillations. How can this can be overcome
6. Draw the electrical equivalent circuit of crystal. and mention its series and parallel resonance frequency?
7. What are the advantages and disadvantages of RC phase shift oscillators?
8. What is the necessary condition for a Wien bridge oscillator circuit to have sustained oscillations?
9. Define piezoelectric effect?
10. What is the principle behind operation of a crystal oscillator?
11. Draw an oscillator circuit with feedback network given below.
12. What are the advantages and disadvantages of wein bridge oscillators?
13. A wein bridge oscillator is used for operations at 9 KHz. If the value of resistance R is 100KΩ, what is the value of C required?
14. A wein bridge oscillator is used for operations at 10 KHz. If the value of resistance R is 100KΩ, what is the value of C required?
15. A tuned collector oscillator in a radio receiver has a fixed inductance of 60μH and has to be tunable over the frequency band of 400 KHz to 1200KHz. Find the range of variable capacitor to be used.
16. Draw the feedback circuit of a colpitts oscillator. Obtain the value of the equivalent series capacitance required if it uses a L of 100mH and is to oscillate at 40KHz.
17. What is the major disadvantage of a Twin-T oscillator?
18. Differentiate oscillator from amplifier.

19. State Barkhausen criterion for sustained oscillation. What will happen to the oscillation if the magnitude of the loop gain is greater than unity?

20. Why an LC tank circuit does not produce sustained oscillations. How can this can be overcome?

21. Draw the electrical equivalent circuit of crystal. and mention its series and parallel resonance frequency.

22. In a Hartley oscillator if L_1=0.2mH,L_2=0.3mH and C=0.003µF. calculate the frequency of its oscillations.
23. In an RC phase shift oscillator, if its frequency of oscillation is 955Hz and R_1=R_2=R_3=680KΩ.Find the value of capacitors.

24. In an RC phase shift oscillator, if R_1=R_2=R_3=200KΩ and C_1=C_2=C_3=100pF. Find the frequency of the oscillator.

25. A crystal has the following parameters L=0.5H, C=0.05pF and mounting capacitance is 2pF. Calculate its series and parallel resonating frequencies.

26. Calculate the frequency of oscillation for the clap oscillator with C_1=0.1µF, C_2=1µF, C_1=100pF and L=470µH.
27. What is the principle behind operation of a crystal oscillator?

28. Draw an oscillator circuit with feedback network given below.

29. What are the advantages and disadvantages of wein bridge oscillators?

30. A wein bridge oscillator is used for operations at 9KHz. If the value of resistance R is 100KΩ, what is the value of C required?

EXPT NO: 5

CURRENT SERIES AND VOLTAGE SERIES FEED BACK AMPLIFIER

AIM: To design a voltage series feedback amplifier with following specifications and to study the frequency response of amplifier, calculate voltage gain and bandwidth from the response.

CIRCUIT DIAGRAM:

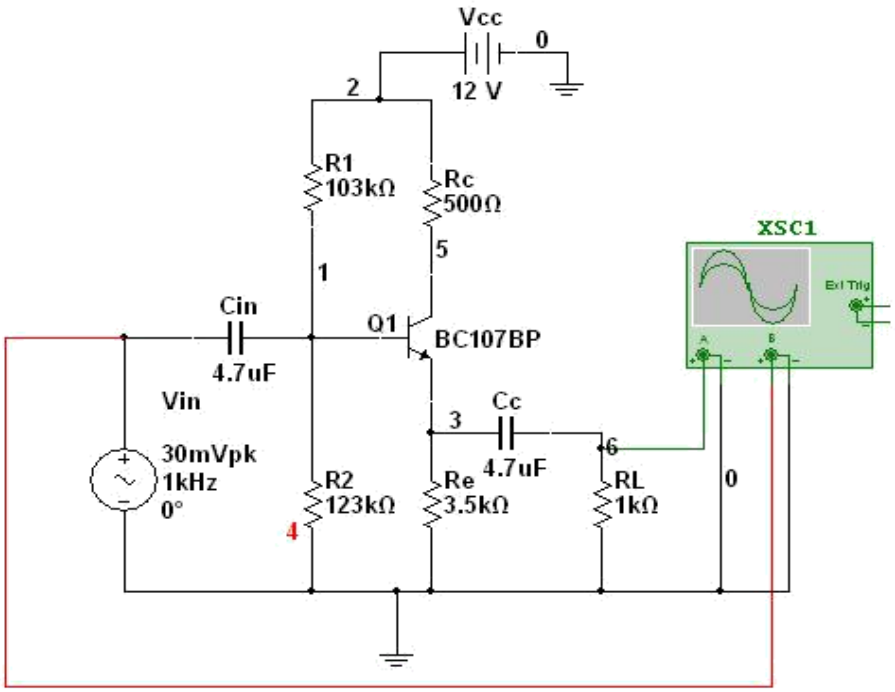


Fig:5. Voltage series feedback Amplifier circuit diagram

DESIGN PROCEDURE:

iv.Determine the R_E using $A_V \quad \frac{h_{fe} x R_E}{R_S \quad h_{ie}} \quad \frac{h_{fe} x R_E}{h_{ie}}$

A_V is calculated as follows

$$A_{Vf} \quad \frac{A_V}{1 A_V} \quad \frac{A_V}{1 A_V} \qquad (1)$$

$A_{Vf} (1 + A_V) = A_V$

$A_{Vf} + A_{Vf} A_V = A_V$

$A_V(1 - A_{Vf}) = A_{Vf}$

$$A_V \quad \frac{A_{Vf}}{1 A_{Vf}}$$

$$A_V \quad \frac{0.995}{1 \ 0.995} 199$$

$$R_E \quad \frac{A_V x h_{ie}}{h_{fe}}$$

$$R_E \quad \frac{199x(22x10^3)}{125} 3502.4$$

$R_E = 3.5$ KΩ

v. Determine the R_C by applying KVL around output loop

$V_{CC} = I_C R_C + V_{CE} + I_C R_E$

$V_{CC} = V_{CE} + I_C (R_C + R_E)$

$12 = 6 + (1.5 \times 10^{-3}) [R_C + 3.5 \times 10^{-3}] R_C = 0.5\ K\Omega$

vi. Determine the R_1 and R_2 as follows

R_1 is calculated using V_{BB} $\frac{R_B}{R_1}$

$$R_1 \frac{V_{CC} x R_B}{V_{BB}}$$

R_B is calculated as follows

Let we know that

$R_I' \ R_B \| R_{If}$

$R_{If} = h_{ie} + h_{fe} \times R_E$

$R_{If} = (22 \times 10^3) + (125 \times 3.5 \times 10^3)$

$R_{If} = 439.7\ K\Omega$

$R_I' \ R_B \| R_{If}$

$$50K \frac{R_B x R_{If}}{R_B \quad R_{If}}$$

$R_B = 56.41\ K\Omega$

V_{BB} is calculated by applying KVL around input loop

$V_{BB} = V_{BE} + I_B R_B + I_E R_E$

$V_{BB} = 0.6 + 0.676 + 5.25 = 6.52$ V

$V_{BB} = 6.52$ V

$$R_1 \quad \frac{V_{CC} X R_B}{V_{BB}}$$

$$R_1 \quad \frac{(12)x(56.41x10_3)}{6.52} \; 103.82K$$

$R_1 = 103.82$ KΩ

$$R_B = \frac{R_1 R_2}{R_1 \quad R_2}$$

$R_2 = 123.59$KΩ

$R_1 = 103.82$ KΩ, $R_2 = 123.59$ KΩ, $R_C = 0.5$ KΩ, $R_E = 3.5$ KΩ

PROCEDURE:

1. Switch ON the computer and open the multisim software.
2. Check whether the icons of the instruments are activated and enable.
3. Now connect the circuit using the designed values of each and every component.
4. Connect the function generator with sine wave of 50 mV p-p as input at the input of terminals of the circuit.
5. Connect the Cathode Ray Oscilloscope (CRO) to the out put terminals of the circuit.
6. Go to simulation button click it for simulation process.
7. From the CRO note the following values
    a. Input voltage V_i =
    b. Output voltage V_0 =
    c. Voltage gain $A_V = V_0/V_i$ =
    d. Phase shift θ =

8. To study the frequency response click the AC analysis, so that a screen displays the following options
    a. Start frequency
    b. Stop frequency
    c. Vertical scale
9. Assign the proper values for start frequency, stop frequency and vertical scale according to the circuit requirements and observe the frequency response.
10. From the frequency response calculate the
    a. maximum gain A_{Vmax} =
    b. lower cutoff frequency (f1) at A_{Vmax} - 3dB (decibel scale) value

        a. at $A_{Vmax}/\sqrt{2}$ (linear scale) =

    c. Higher cutoff frequency (f2) at A_{Vmax} - 3dB (decibel scale) value

RESULT: -

1. Frequency response of Voltage Series Feed Back amplifier is plotted.
2. Gain = _____dB (maximum).
3. Bandwidth= f_H-f_L = _____Hz.

APPLICATIONS:

1. Voltage series feedback (Af= Vo/Vs) –Voltage amplifier
2. Voltage shunt feedback (Af= Vo/Is) –Trans-resistance amplifier
3. Current series feedback (Af= Io/Vs) -Trans-conductance amplifier
4. Current shunt feedback (Af= Io/Is) -Current amplifier

EXERCISE PROBLEMS:

1. Plot the frequency and amplitude response of BC 107 amplifier with C_1 = 5 µF.
2. Plot the frequency response of BC 107amplifier with C_2 = 5 µF with triangular i/p.
3. Plot the amplitude response of BC 107 amplifier with R_1 = 4.1 K.
4. Plot the amplitude response of BC 107 amplifier with R_2 = 9.4 K triangular i/p.
5. Plot frequency response of BC 107 amplifier R_1 = 4.1 K, R_2 = 9.4 K with square i/p.
6. Plot the frequency and amplitude response of BC 107 amplifier with C_1 = 5 µF.
7. Plot the frequency response of amplifier with C_2 = 5 µF, triangular i/p.
8. Plot the amplitude response of BC 107 amplifier with R_1 = 4.1 K.
9. Plot the amplitude response of BC107 amplifier with R_2 = 9.4 K triangular i/p.
10. Plot frequency response of BC107 R1 = 4.1 K, R_2 = 9.4 K with square i/p.
11. Plot the frequency and amplitude response of BC107 amplifier with C_1 = 10 µF.
12. Plot the frequency response of BC 107amplifier with C_2 = 2 µF with i/p.
13. Plot the amplitude response of BC 107 amplifier with R_1 = 2.1 K.
14. Plot the amplitude response of BC 10 7amplifier with R_2 = 5.4 K i/p.
15. Plot frequency response of BC 107amplifier R_1 = 2.1 K, R_2 = 2.4 K with i/p.
16. Plot the frequency and amplitude response of BC 107amplifier with C_1 = 2 µF.
17. Plot the frequency response of amplifier with C_2 = 2 µF, i/p.
18. Plot the amplitude response of BC 107 amplifier with R_1 = 2.1 K.
19. Plot the amplitude response of BC 107 amplifier with R_2 = 2.4 K i/p.
20. Plot frequency response of R1 = 2.1 K, R_2 = 9.4 K with i/p.
21. Plot the frequency and amplitude response of BC 107 amplifier with C_1 = 5 µF.
22. Plot the frequency response of BC 107 amplifier with C_2 = 5 µF with i/p.
23. Plot the amplitude response of BC 107 amplifier with R_1 = 4.1 K.
24. Plot the amplitude response of BC 107 amplifier with R_2 = 9.4 K i/p.
25. Plot frequency response of BC 107amplifier R_1 = 4.1 K, R_2 = 9.4 K with i/p.
26. Plot the frequency and amplitude response of BC 107 amplifier with C_1 = 5 µF.
27. Plot the frequency response of amplifier with C_2 = 5 µF, i/p.
28. Plot the amplitude response of BC107 amplifier with R_1 = 4.1 K.
29. Plot the amplitude response of BC 107 amplifier with R_2 = 9.4 K i/p.
30. Plot frequency response of R1 = 4.1 K, R_2 = 9.4 K with i/p

VIVA QUESTIONS:

1. State the merits and demerits of negative feedback in amplifiers.
2. If the bypass capacitor C_E in an RC coupled amplifier becomes accidentally open circuited, what happens to the gain of the amplifier? Explain.
3. When will a negative feedback amplifier circuit be unstable?
4. What is the parameter which does not change with feedback?
5. What type of feedback has been used in an emitter follower circuit?
6. Define voltage series feedback amplifier?
7. Draw the voltage series feedback amplifier?
8. When will a negative feedback amplifier circuit be unstable?
9. What is the parameter which does not change with feedback?
10. What type of feedback has been used in an emitter follower circuit?

11. Transistor when it is working as an amplifier?
12. Why frequency response of the amplifier is drawn on semi-log scale graph?
13. If Q point is not properly selected, then what will be the effect on the output waveform?
14. What is active region?
15. Why is common base configuration used as current buffer even though it has properties of current amplifier?
16. What does the current shunt feedback amplifier amplify? And how?
17. If the bypass capacitor C_E in an RC coupled amplifier becomes accidentally open circuited,
18. What happens to the gain of the amplifier? Explain.
19. When will a negative feedback amplifier circuit be unstable?
20. What is the parameter which does not change with feedback?
21. Transistor when it is working as an amplifier?
22. Why frequency response of the amplifier is drawn on semi-log scale graph?
23. If Q point is not properly selected, then what will be the effect on the output waveform?
24. What is active region?
25. What is Bandwidth of an amplifier?
26. Why is common base configuration used as current buffer even though it has properties of current amplifier?
27. State the merits and demerits of negative feedback in amplifiers.
28. If the bypass capacitor C_E in an RC coupled amplifier becomes accidentally open Circuited, what happens to the gain of the amplifier? Explain.
29. Define voltage series feedback amplifier?
30. What is Bandwidth of an amplifier?

EXPT NO: 6

COLPITTS AND HARTLEY OSCILLATOR

AIM:

Find practical frequency of Colpitt's oscillator and to compare it with theoretical Frequency for L= 5mH and C= 0.001 F, 0.0022 F, 0.0033 F respectively.

COMPONENTS & EQIUPMENT REQUIRED: -

S.No	Device	Range/Rating	Quantity
1	a) DC supply voltage b) Inductors c) Capacitor d) Resistor e) NPN Transistor	12V 5mH 0.01 F,0.01 F,100 F 1K ,10K ,47K BC 107	1 1 1 1 1
2	Cathode Ray Oscilloscope	(0-20) MHz	1
3.	BNC Connector		1
4	Connecting wires	5A	4

CIRCUIT DIAGRAM:

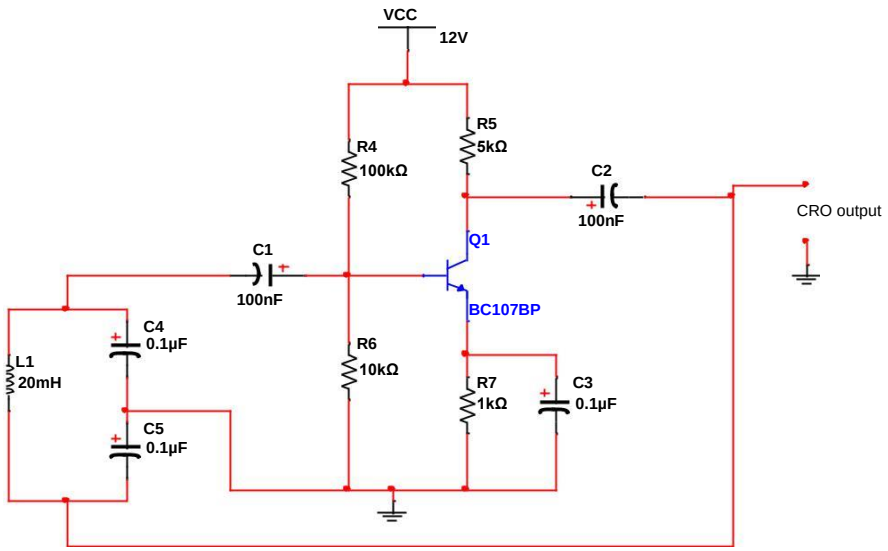


Fig: 6.1 Colpitts oscillator circuit diagram

PROCEDURE:-

1. Connect the circuit as shown in the figure
2. Connect C_2= 0.001 Fin the circuit and observe the waveform.
3. Time period of the waveform is to be noted and frequency should be calculated by the formula f=1/T
4. Now, fix the capacitance to 0.002 F and then to 0.003 F and calculate the frequency and tabulate the reading as shown.
5. Find theoretical frequency from the formula f= $\frac{1}{2\sqrt{LC_T}}$

Where C_T $\frac{C_1 C_2}{C_1 C_2}$ and compare theoretical and practical values.

PRECAUTIONS:-

1. No loose connections at the junctions.

TABULAR COLUMN:

S.NO	L(mH)	C_1 (F)	C_2 (F)	C_T (F)	Theoretical Frequency (KHz)	Practical Frequency (KHz)	Vo(V) Peak to peak
1	1mH	.1u	0.1u				
2	1mH	0.01u	0.1u				
3	1mH	0.01	0.0iu				

RESULT:

1. For C=0.01 F, 0.1uf & L= 1mH
   Theoretical frequency =
   Practical frequency =
2. For C=0.1 F, 0.1uf & L= 1mH

3. For C=0.01 F, 0.01uf & L= 5mH
   Theoretical frequency =
   Practical frequency =

HARTLEY OSCILLATOR

AIM:

Find practical frequency of a Hartley oscillator and to compare it with theoretical frequency for L = 10mH and C = 0.01 F, 0.033 F and 0.047 F.

COMPONENTS AND EQUIPMENTS REQUIRED:

S.No	Device	Range/Rating	Quantity
1	a) DC supply voltage b) Inductors c) Capacitor d) Resistor e) NPN Transistor	12V 5mH 0.01 F,0.022 F;0.033 F 0.047 F 1K ,10K ,47K BC 107	1 2 1 1 1 1
2	Cathode Ray Oscilloscope	(0-20) MHz	1
3.	BNC Connector		1
4	Connecting wires	5A	4

CIRCUIT DIAGRAM:

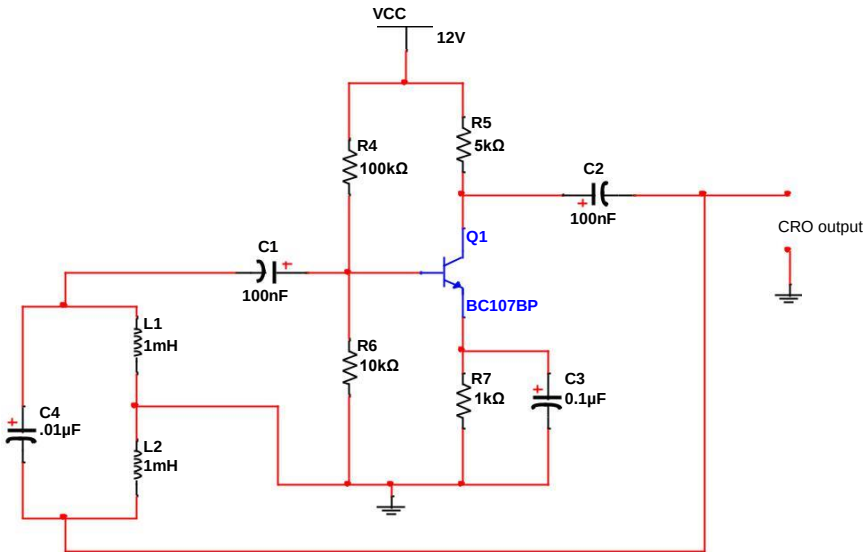


Fig: 6.2 Hartley oscillator circuit diagram

PROCEDURE:

1. Connect the circuit as shown in figure.
2. With 0.1 F capacitor and 20mH in the circuit and observe the waveform.
3. Time period of the waveform is to be noted and frequency is to be calculated by the formula f = 1/T .
4. Now fix the capacitance to 0.033 F and 0.047 F and calculate the frequency and tabulate the readings as shown.
5. Find the theoretical frequency from the formula $f = \frac{1}{2\sqrt{L_T C}}$ ——— Where $L_T = L_1 + L_2 = 5mH + 5mH = 10mH$ and compare theoretical and practical values.

PRECAUTIONS: No loose contacts at the junctions.

TABULATIONS:

S.No	L_T(mH)	C (F)	Theoretical frequency (KHz)	Practical frequency (KHz)	V_o (peak to peak)
1	10	0.01			
2	10	0.033			
3	10	0.047			

RESULT:

1. For C = 0.01 F, & L_T = 10 mH;
   Theoretical frequency
   = Practical frequency =
2. For C = 0.033 F, & L_T = 10 mH;
   Theoretical frequency =
   Practical frequency =
3. For C = 0.047 F, & L_{Ts} = 10 mH;
   Theoretical frequency =
   Practical frequency =

APPLICATIONS:

1. It is used for generation of sinusoidal output signals with very high frequencies.
2. The Colpitts oscillator using SAW device can be used as the different type of sensors such as temperature sensor. As the device used in this circuit is highly sensitive to perturbations, it senses directly from its surface.
3. It is frequently used for the applications in which very wide range of frequencies are involved.
4. The Hartley oscillator is to produce a sine wave with the desired frequency
5. Hartley oscillators are mainly used as radio receivers. Also note that due to its wide range of frequencies, it is the most popular oscillator
6. The Hartley oscillator is Suitable for oscillations in RF (Radio-Frequency) range, up to 30MHZ

VIVA QUESTIONS:

1. Give the difference between Hartley and colpitts oscillator.
2. Classification of oscillators.
3. Give an example for LC oscillator.
4. Which phenomenon is employed for colpitts oscillator?
5. Give the applications of oscillator.
6. Define barkhausen criteria
7. Which type of feedback is employed in oscillators
8. Give applications for oscillators
9. What is the condition for sustained oscillations
10. Draw an oscillator circuit with feedback network given below.
11. What is the principle behind operation of a colpits oscillator?
12. What are the advantages and disadvantages of *colpits* oscillators?
13. Mention two essential conditions for a circuit to maintain oscillations?
14. Define an oscillator?
15. Which feedback used in oscillators?
16. Classify oscillators?
17. which oscillators are AF oscillators?
18. Draw an oscillator circuit with feedback network given below.
19. What is the principle behind operation of a *HARTLEY* oscillator?
20. What are the advantages and disadvantages of *HARTLEY* oscillators?
21. Mention two essential conditions for a circuit to maintain oscillations[
22. Define an oscillator?
23. Define barkhausen criteria
24. What are RC oscillators?
25. Mention two essential conditions for a circuit to maintain oscillations[
26. Define an oscillator?
27. Define barkhausen criteria
28. Which type of feedback is employed in oscillators
29. Give applications for oscillators
30. Which oscillators are AF oscillators?

EXERCISE PROBLEMS:

1. Plot the Amplitude response of 2N3904 Oscillator with C_1 = 5 µF.
2. Plot the Amplitude response of 2N2222 Oscillator C2 = 5 µF with i/p.
3. Plot the Amplitude response of BC107 Oscillator with R_1 = 4.1 K.
4. Plot the Amplitude response of BC 547 Oscillator with R_2 = 9.4 K i/p.
5. Plot the Amplitude response of BC 548 Oscillator R1 = 4.1 K, R_2 = 9.4 K with i/p.
6. Plot the Amplitude response of BC 557 Oscillator with C_1 = 5 µF.
7. Plot the Amplitude response of BC 547 Oscillator with C_2 = 5 µF, i/p.
8. Plot the Amplitude response of 2N3904 Oscillator with R_1 = 4.1 K.
9. Plot the Amplitude response of 2N3904 Oscillator with R_2 = 9.4 K i/p.
10. Plot the Amplitude response of 2N3904 Oscillator R1 = 4.1 K, R_2 = 9.4 K with i/p.
11. Plot the Amplitude response of 2N3904 Oscillator with C_1 = 10 µF.
12. Plot the Amplitude response of CL100 Oscillator with C_2 = 2 µF with i/p.
13. Plot the Amplitude response of CL 100 Oscillator with R_1 = 2.1 K.
14. Plot the Amplitude response of CK 100 Oscillator with R_2 = 5.4 K i/p

15. Plot the Amplitude response of 2N3904 Oscillator with C_1 = 5 µF.
16. Plot the Amplitude response of 2N2222 Oscillator C2 = 5 µF with i/p.
17. Plot the Amplitude response of BC107 Oscillator with R_1 = 4.1 K.
18. Plot the Amplitude response of BC 547 Oscillator with R_2 = 9.4 K i/p.
19. Plot the Amplitude response of BC 548 Oscillator R1 = 4.1 K, R_2 = 9.4 K with i/p.
20. Plot the Amplitude response of BC 557 Oscillator with C_1 = 5 µF.
21. Plot the Amplitude response of BC 547 Oscillator with C_2 = 5 µF, i/p.
22. Plot the Amplitude response of 2N3904 Oscillator with R_1 = 4.1 K.
23. Plot the Amplitude response of 2N3904 Oscillator with R_2 = 9.4 K i/p.
24. Plot the Amplitude response of 2N3904 Oscillator R1 = 4.1 K, R_2 = 9.4 K with i/p.
25. Plot the Amplitude response of 2N3904 Oscillator with C_1 = 10 µF.
26. Plot the Amplitude response of CL100 Oscillator with C_2 = 2 µF with i/p.
27. Plot the Amplitude response of CL 100 Oscillator with R_1 = 2.1 K.
28. Plot the Amplitude response of CK 100 Oscillator with R_2 = 5.4 K i/p.
29. Plot the Amplitude response of 2N3904 Oscillator R1 = 2.1 K, R_2 = 2.4 K with i/p.

EXPT NO: 7

DOUBLE STAGE RC COUPLED AMPLIFIER

AIM: -

1. Plot the frequency response of a Two Stage Amplifier.
2. Calculate gain.
3. Calculate bandwidth.

COMPONENTS & EQUIPMENTS REQUIRED: -

S.No	Device	Range/Rating	QTY
1.	(a) DC supply voltage	12V	1
	(b) Transistor	BC107	1
	(c) Capacitors	10 F	2
		100 F	1
	(d) Resistors	100 ,470	1
		4.7K ,8.2k	1
2.	Signal generator	0.1Hz-1MHz	1
3.	CRO	0Hz-20MHz	1
4.	Connecting wires	5A	4

CIRCUIT DIAGRAM:

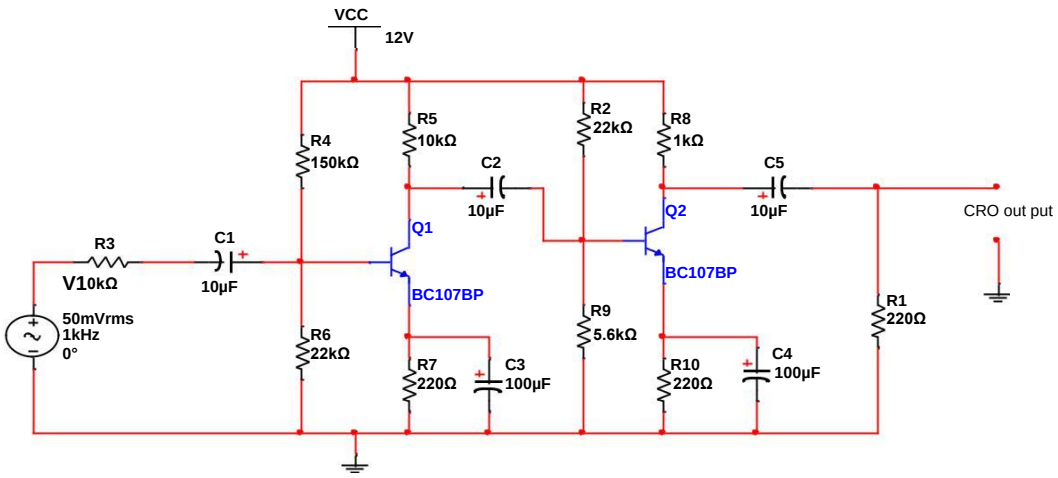


Fig: 7 Two Stages RC coupled amplifier circuit

PROCEDURE: -

1. Connect the circuit diagram as shown in figure.
2. Adjust input signal amplitude in the function generator and observe an amplified voltage at the output without distortion.
3. By keeping input signal voltage, say at 50mV, vary the input signal frequency from 0 to 1MHz in steps as shown in tabular column and note the corresponding output voltages.

PRECAUTIONS:

Avoid loose connections and give proper input Voltage

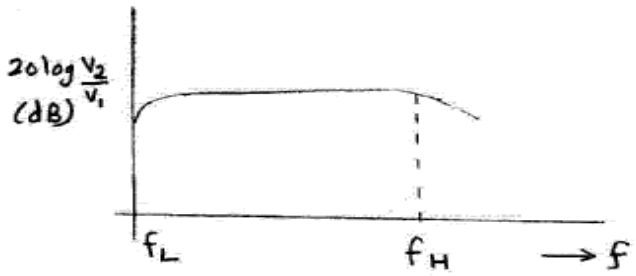
TABULAR COLUMN: **Input = 50mV**

Frequency(in Hz)	Output Voltage (V_o)		Gain $A_v=V_o/V_i$		Gain(in dB) $=20\log_{10}(V_o/V_i)$	
	With feedback	Without feedback	With feedback	Without feedback	With feedback	Without feedback
20						
40						
80						
100						
1K						
10k						
50k,100K						
1M						

RESULT: -

1. Frequency response of Two stage RC coupled amplifier is plotted.
2. Gain = _____dB (maximum).
3. Bandwidth= f_H-f_L = _____Hz. At stage I
4. Bandwidth= f_H-f_L = _____Hz. At stage 2

EXPECTED GRAPH:



APPLICATIONS:

1. They are widely used as voltage amplifiers (ie. In the initial stages of public address systems) because of their excellent audio-fidelity over a wide range of frequency. However because of poor impedance matching this type of coupling transistor circuits is rarely employed in final stages impedance matching voltage amplifier in initial stage of public addressing system.

2. To increase the power gain, high input impedance, low output impedance, and increase the weaken signal.

3. To increase the power gain, high input impedance, low output impedance, and increase the weaken signal.

4. In a two stage RC coupled amplifier, the two transistors are identical and a common power supply is used. The input is provided to the first stage of the amplifier where it is amplified and this output is used as input for the second stage.

5. This is amplified once again by the other transistor in the second stage and the final output is obtained.

6. There will be a 180 degree phase shift after the first stage amplification which is nullified by the 180 degree phase shift of the second stage amplification. Thus, we obtain an output which is an amplified signal of the input and is in phase with the input signal.

VIVA QUESTIONS:

1. Why do you need more than one stage of amplifiers in practical circuits?
2. What is the effect of cascading on gain and bandwidth?
3. What happens to the 3dB frequencies if the number of stages of amplifiers increases?
4. Why we use a logarithmic scale to denote voltage or power gains, instead of using the simpler linear scale?
5. What is loading effect in multistage amplifiers?
6. What is the necessity of cascading?
7. What is 3dB bandwidth?
8. Why RC coupling is preferred in audio range?
9. Which type of coupling is preferred and why?
10. Explain various types of Capacitors?
11. What is loading effect?
12. Why it is known as RC coupling?
13. What is the purpose of emitter bypass capacitor?
14. Which type of biasing is used in RC coupled amplifier?
15. What is difference between Amplifier and Attenuator?
16. Which Amplifier will amplify voltage and current?
17. What are the advantages over single stage amplifier?
18. What are the classifications of multistage amplifiers?
19. What are the different BJT multistage amplifier configurations?
20. Define cut off frequency?
21. What Is the pin configuration on bread board used in the lab?
22. What is two stages RC coupled amplifier?
23. Which type of coupling is preferred and why?
24. Explain various types of Capacitors?
25. What is loading effect?
26. Why it is known as RC coupling?
27. What is the purpose of emitter bypass capacitor?
28. Which type of biasing is used in RC coupled amplifier?
30. What is two stages RC coupled amplifier?

EXERCISE PROBLEMS:

1. Plot the frequency response of BC 107 amplifier with C_1 = 5 µF.
2. Plot the frequency response of BC 547 amplifier with C_2 = 5 µF with i/p.
3. Plot the frequency response of BC 2N2222 amplifier with R_1 = 4.1 K.
4. Plot the frequency response of BC 107 amplifier with R_2 = 9.4 K i/p.
5. Plot frequency response of BC 107 amplifier R_1 = 4.1 K, R_2 = 9.4 K with i/p.
6. Plot the frequency and amplitude response of BC 107 amplifier with C_1 = 5 µF.
7. Plot the frequency response of amplifier with C_2 = 5 µF, i/p.
8. Plot the frequency response of BC 107 amplifier with R_1 = 4.1 K.
9. Plot the frequency response of BC107 amplifier with R_2 = 9.4 K i/p.
10. Plot frequency response of BC107 R1 = 4.1 K, R_2 = 9.4 K with i/p.
11. Plot the frequency and amplitude response of BC107 amplifier with C_1 = 10 µF.
12. Plot the frequency response of BC 107amplifier with C_2 = 2 µF with i/p.
13. Plot the frequency response of BC 107 amplifier with R_1 = 2.1 K.
14. Plot the frequency response of BC 10 7amplifier with R_2 = 5.4 K i/p.
15. Plot frequency response of BC 107amplifier R_1 = 2.1 K, R_2 = 2.4 K with i/p.
16. Plot the frequency and amplitude response of BC 107amplifier with C_1 = 2 µF.
17. Plot the frequency response of amplifier with C_2 = 2 µF, i/p.
18. Plot the frequency response of BC 107 amplifier with R_1 = 2.1 K.
19. Plot the frequency response of BC 107 amplifier with R_2 = 2.4 K i/p.
20. Plot frequency response of R1 = 2.1 K, R_2 = 9.4 K with i/p.
21. Plot the frequency response of BC 107 amplifier with C_1 = 5 µF.
22. Plot the frequency response of BC 107 amplifier with C_2 = 5 µF with i/p.
23. Plot the frequency response of BC 107 amplifier with R_1 = 4.1 K.
24. Plot the frequency response BC 107 amplifier with R_2 = 9.4 K i/p.
25. Plot frequency response of BC 107amplifier R_1 = 4.1 K, R_2 = 9.4 K with i/p.
26. Plot the frequency and amplitude response of BC 107 amplifier with C_1 = 5 µF.
27. Plot the frequency response of amplifier with C_2 = 5 µF, i/p.
28. Plot the frequency response of BC107 amplifier with R_1 = 4.1 K.
29. Plot the frequency response of BC 107 amplifier with R_2 = 9.4 K i/p.
30. Plot frequency response of R_1 = 4.1 K, R_2 = 9.4 K with i/p

EXPT NO: 8

CLIPPERS AND CLAMPPERS

AIM:

To study the clipping circuits for different reference voltages and to verify the responses.

COMPONENTS REQUIRED:

1. Resistors - 1KΩ
2. IN4007 Diode – 2No.

APPARATUS REQUIRED:

1. Bread board.
2. CRO (1Hz – 20MHz)
3. Function Generator(1Hz-1MHz)
4. Power supply(0-30V)
5. Connecting wires.

THEORY:

The non-linear semiconductor diode in combination with resistor can function as clipper circuit. Energy storage circuit components are not required in the basic process of clipping.

These circuits will select part of an arbitrary waveform which lies above or below some particular reference voltage level and that selected part of the waveform is used for transmission. So they are referred as voltage limiters, current limiters, amplitude selectors or slicers.

There are three different types of clipping circuits.

1) Positive Clipping circuit.

2) Negative Clipping.

3) Positive and Negative Clipping (slicer).

In positive clipping circuit positive cycle of Sinusoidal signal is clipped and negative portion of sinusoidal signal is obtained in the output of reference voltage is added, instead of complete positive cycle that portion of the positive cycle which is above the reference voltage value is clipped.

In negative clipping circuit instead of positive portion of sinusoidal signal, negative portion is clipped.

In slicer both positive and negative portions of the sinusoidal signal are clipped.

I. Positive Clipping

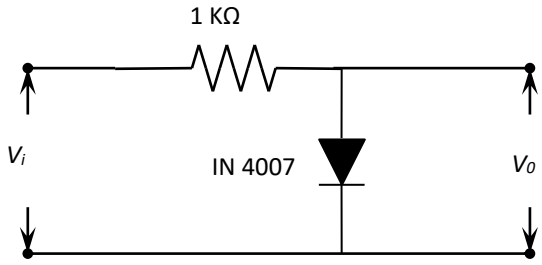


Figure:1

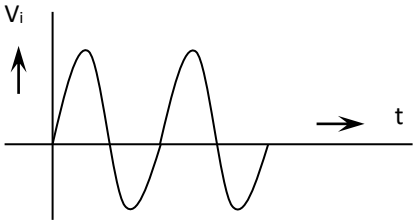


Figure: 1(a). Input waveform

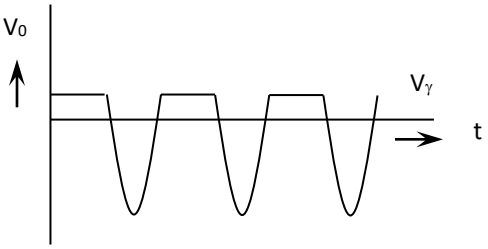


Figure: 1(b) Output waveform.

V_i is a input sinusoidal signal as shown in the figure 1(a) . For positive portion of the sinusoidal the diode IN4007 gets forward biased. The output voltages in the voltage across the diode under forward biased which is cut-in-voltage of the diode. Therefore the positive portion above the cut-in-voltage is clipped or not observed in the output *(V_0)* as shown in figure 1(b).

II. Positive Clipping with Positive Reference Voltage

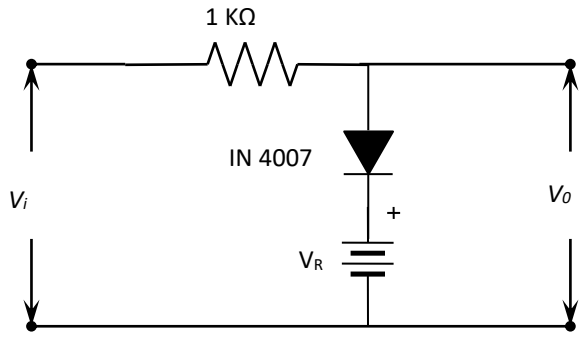


Figure: 2.

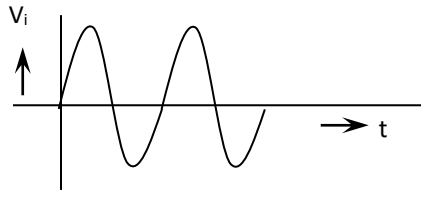


Figure:2(a). Input waveform

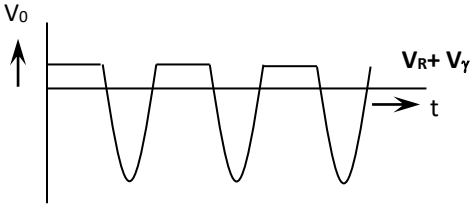


Figure:2(b).Output waveform.

The input sinusoidal signal (V_i) in figure 1(a) can make the diode to conduct when its instantaneous value is greater than V_R. Up to that voltage (V_R) the diode is open circuited and the output voltage is same as the input voltage. After that voltage (V_R) the output voltage is V_R plus the cut-in-voltage (V_γ) of the diode as shown in figure 2(b).

III. Positive Clipping with Negative Reference Voltage

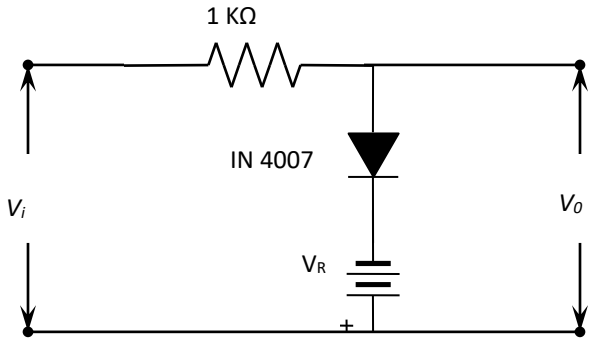


Figure: 3

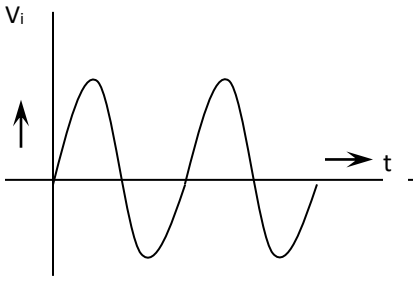


Figure:3(a). Input waveform

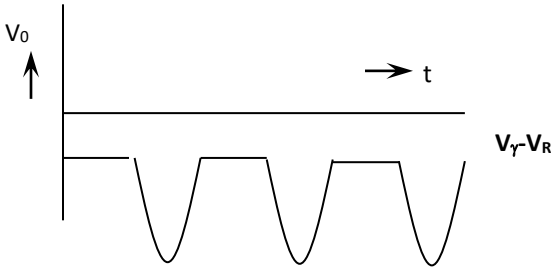


Figure:3(b) Output waveform.

In this circuit the diode conducts the output voltage is same as input voltage. The diode conducts at a voltage less by V_R from cut-in-voltage called as V_γ. For voltage less than V_γ, the diode is open circuited and output is same as input voltage.

IV Negative Clipping Circuit

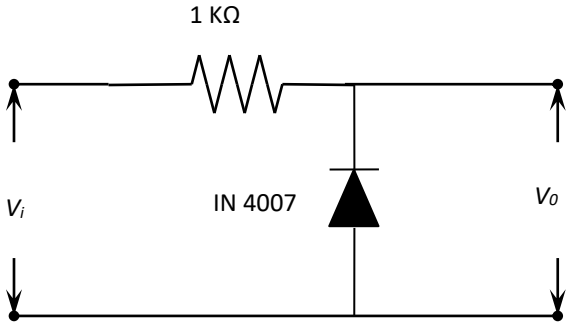


Figure:4

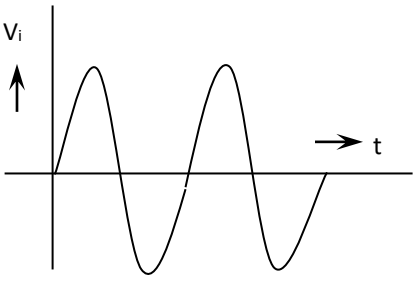


Figure:4 (a). Input waveform

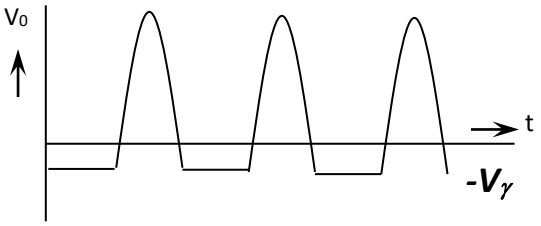


Figure:4 (b). Output waveform.

For this portion of the input sinusoidal signal *(Vi)*, the diode gets reverse biased and it is open. Then the output voltage is same as input voltage. For the negative portion of the signal the diode gets forward biased and the output voltage is the cut-in-voltage *(-V_γ)* of the diode. Then the input sinusoidal variation is not seen in the output. Therefore the negative portion of the input sinusoidal signal *(Vi)* is clipped in the output signal *(V_0)*.

V. <u>Negative Clipping with Negative Reference Voltage</u>

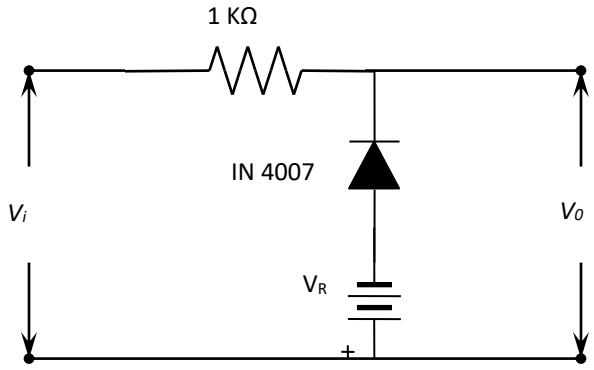


Figure:5

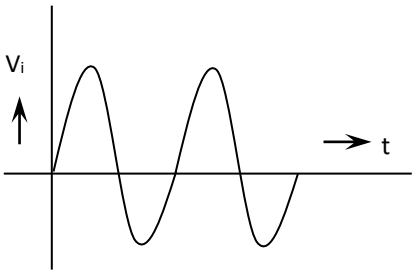


Figure:5(a). Input waveform.

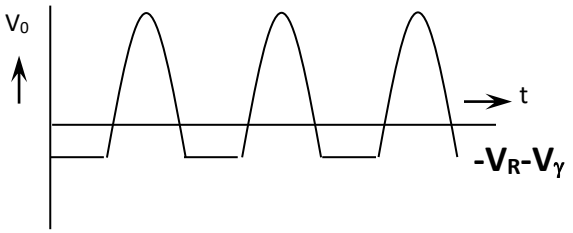


Figure:5(b) Output waveform.

In this circuit, the diode gets forward biased for the input sinusoidal voltage is less than ($-V_R$). For input voltage greater than ($-V_R$), the diode is non-conducting and it is open. Then the output voltage is same as input voltage.

VI. <u>Negative Clipping with Positive Reference Voltage</u>

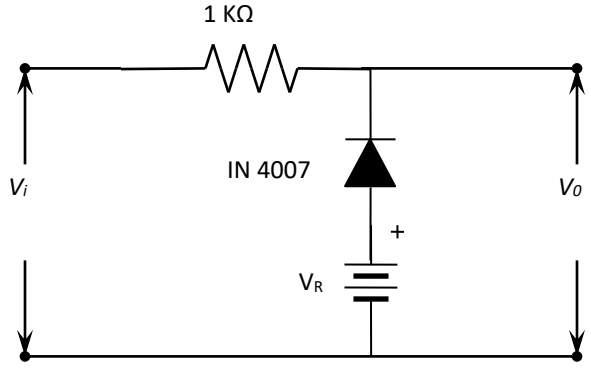


Figure: 6

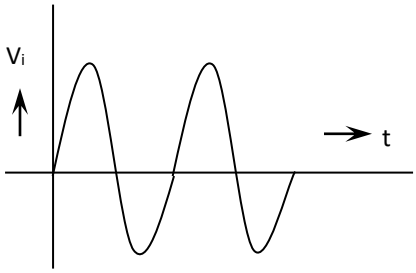


Figure:6(a) Input waveform

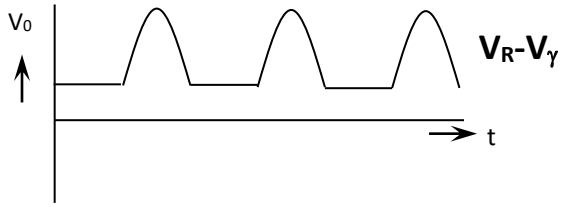


Figure:6(b) Output waveform.

For input sinusoidal signal voltage less than V_R, the diode is shorted and the output voltage is fixed arV_R. For input sinusoidal voltage greater than V_R the diode is reverse biased and open circuited. Then the output voltage is same as input voltage.

VII. Slicer

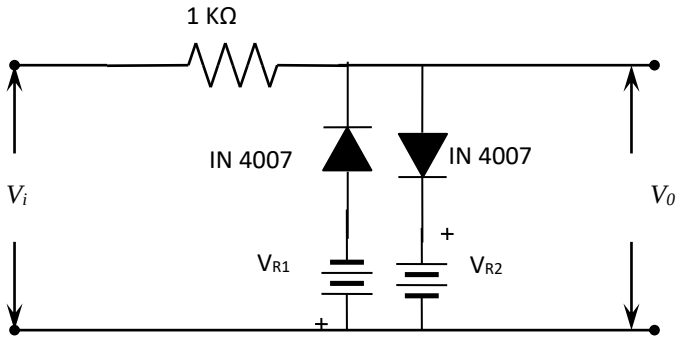


Figure:7

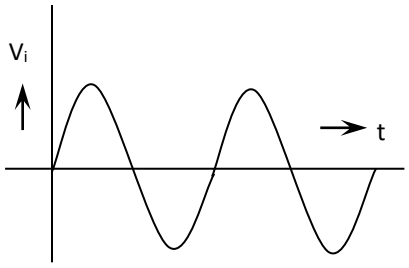


Figure:7(a). Input waveform

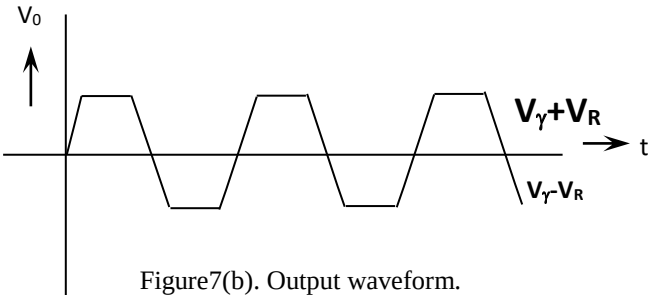


Figure7(b). Output waveform.

OBSERVATION TABLE:

S.No	Type of Clipping	Vin	$V_\gamma \pm V_R$	Theoretical Calculation Vclipped=Vin-Vout	Practical Calculation
1					
2					
3					

DESIGN:

1. For positive clipping at 'V' volts reference select $V_R = V$.
2. For negative clipping at 'V' volts reference select $V_R = V$.
3. For clipping at two independent levels at V_1&V_2 reference voltages select $V_{R1} = V_1$, $V_{R2} = V_2$ and $V_{R2} = V_{R1}$.

PROCEDURE:

1. Connect the circuit as shown in the figure 1.
2. Connect the function generator at the input terminals and CRO at the output terminals of the circuit.
3. Apply a sine wave signal of frequency 1KHz, Amplitude greater than the reference voltage at the input and observe the output waveforms of the circuits.

CONCLUSION:

Conclusion can be made on theoretical and practical values of cut in voltage of diode and also made on theoretical and practical output wave forms for different reference voltages

CLAMPPERS

AIM :

To study the clampling circuits for different referencevoltages and to verify the responses.

COMPONENTS REQUIRED:

1. Resistors - 1kΩ
2. IN4007 Diode
3. Capacitor -10μF

APPARATUS REQUIRED:

1. Bread board
2. Function generator (1Hz – 1Mz)
3. CRO (1Hz- 20MHz)
4. Power supply (0-30V)
5. Connecting Wires.

THEORY:

Clamping Circuit

"A clamping circuit is one that takes an input waveform and provides an output that is a faithful replica of its shape but has one edge tightly clamped to the zero voltage reference point".

There are various types of Clamping circuits, which are mentioned below:

1. Positive Clamping Circuit.
2. Negative Clamping Circuit.
3. Positive Clamping with positive reference voltage.
4. Negative Clamping with positive reference voltage.
5. Positive Clamping with negative reference voltage.
6. Negative Clamping with negative reference voltage.

Negative Clamping Circuit

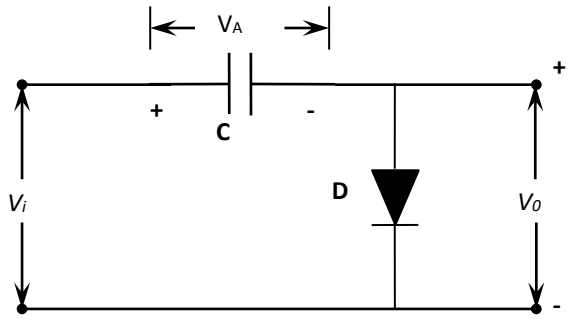


Figure:1

The input signal is a sinusoidal which begins at t=0. The capacitor C is charged at $t = 0$. The waveform across the diode at various instant is studied.

During the first quarter cycle the input signal rises from zero to the maximum value V_m. The diode being ideal, no forward voltage may appear across it. During this first quarter cycle the capacitor voltage $V_A = V_i$. The voltage across C rises sinusoidally, the capacitor is charged through the series combination of the signal source and the diode. Throughout this first quarter cycle the output V_0 has remained zero. At the end of this quarter cycle there exists across the capacitor a voltage $V_A = V_m$.

After the first quarter cycle, the peak has been passed and the input signal begins to fall, the voltage V_A across the capacitor is no longer able to follow the input voltage. For in order to do so, it would be required that the capacitor discharge, and because of the diode, such a discharge is not possible. The capacitor remains charged to the voltage $V_A = V_m$, and, after the first quarter cycle the output is $V_0 = V_i - V_m$. During succeeding cycles the positive excursion of the signal just barely reaches zero. The diode need never again conduct, and the positive extremity of the signal has been clamped to zero. The average value of the signal is $-V_m$.

Positive Clamping Circuit:

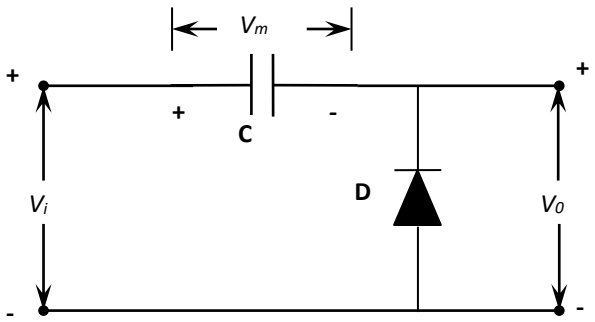


Figure:2

It is also called as negative peak clamper, because this circuit clamps at the negative peaks of a signal.

Let the input signal be $V_i = V_m \sin\omega t$. When V_i goes negative, diode gets forward biased and conducts. The capacitor charges to voltage V_m, with polarity as shown. Under steady state condition, the positive clamping circuit is given as,

$$V_0 = V_i - (-V_m)$$

$$\boxed{V_0 = V_i + V_m} \qquad \text{Eq.1}$$

During the negative half cycle of V_i, the diode conducts and C charges to $-V_m$ volts, i.e., the negative peak value. The capacitor cannot discharge since the diode cannot conduct in the reverse direction. Thus the capacitor acts as a battery of $-V_m$ volts and the output voltage is given by equation.1 above. It is seen for figure 2, that the negative peaks of the input signal are clamped to zero level. Peak-to-peak amplitude of output voltage $2V_m$, which is the same as that of the input signal.

Negative Clamping with Positive Reference Voltage

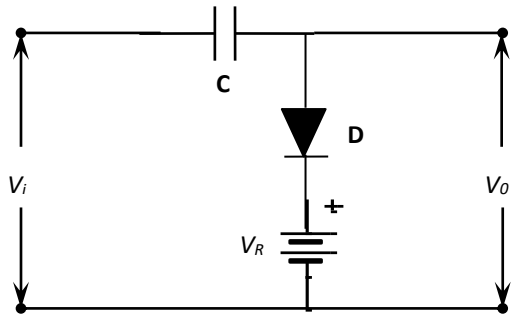


Figure:3

Since V_R is in series with the output of negative clamping circuit, now the average value of the output becomes $(-V_m + V_R)$.

Similarly, the average of

i) Negative clamping with negative reference voltage is $(-V_m + V_R)$.

ii) Positive clamping is $+V_m$.

iii) Positive clamping with positive reference voltage is $V_m + V_R$.

iv) Positive clamping with negative reference voltage is $V_m - V_R$.

Clamping Circuit Theorem:

It states that for any input waveform the ratio of the areas under the output voltage curve in forward direction to that in the reverse direction is equal to the ratio (R_f / R).

$$\frac{A_f}{A_r} = \frac{R_f}{R}.$$

Where A_f = area of the output wave in forward direction.

A_r = area of the output wave in reverse direction.

$Rf$and$R$ are forward and reverse resistances of the diode.

I. <u>Negative Clamping</u>

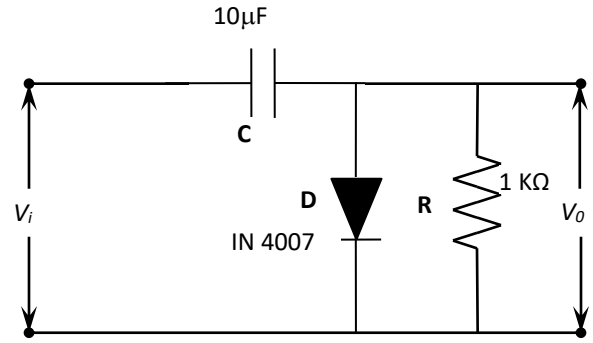


Figure:4

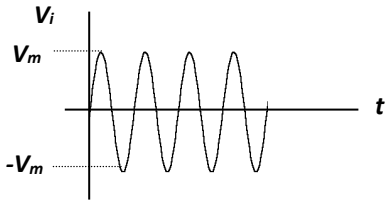


Figure:4 (a).Input waveform

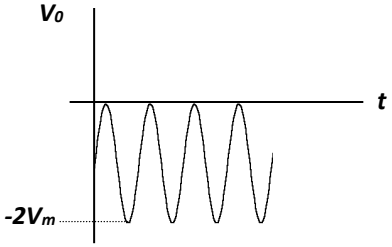


Figure: 4 (b) Output waveform.

II. <u>Negative Clamping with Positive Reference Voltage.</u>

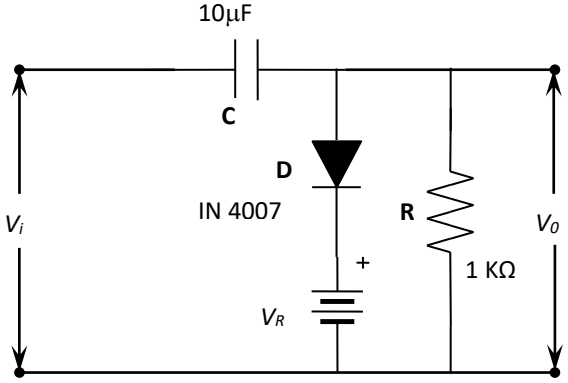


Figure:5

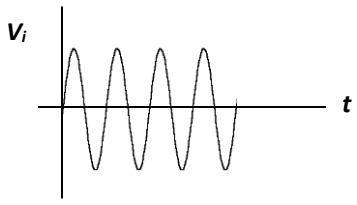


Figure:6 (a).Input waveform

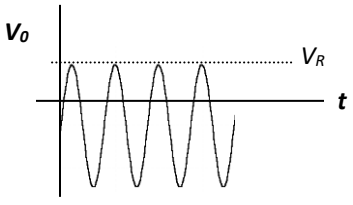


Figure:6 (b) Output waveform.

III. <u>Negative Clamping with Negative Reference Voltage.</u>

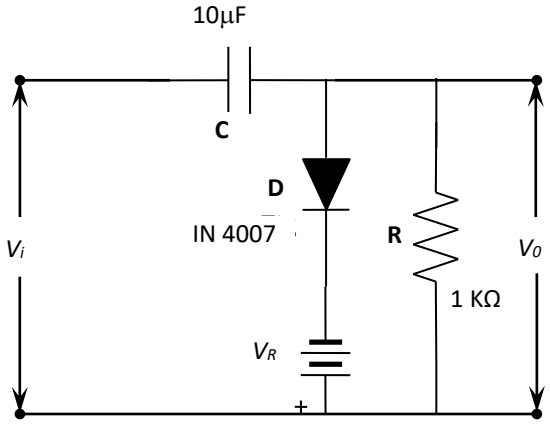


figure:7

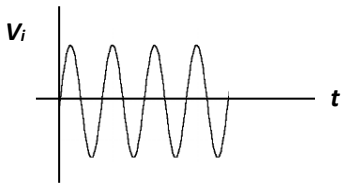


Figure:7 (a).Input waveform

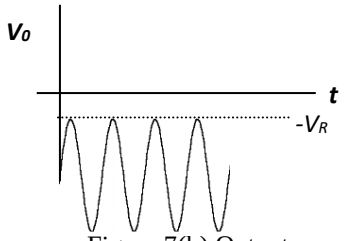


Figure:7(b) Output waveform.

IV. <u>Positive Clamping.</u>

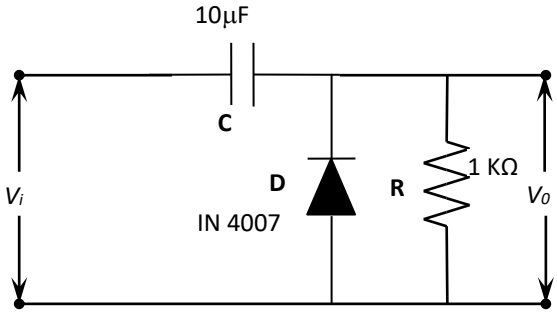


figure:8

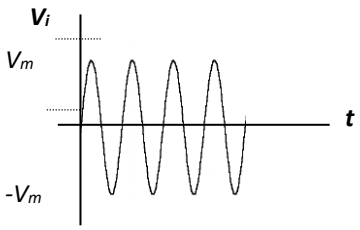


Figure:8 (a).Input waveform

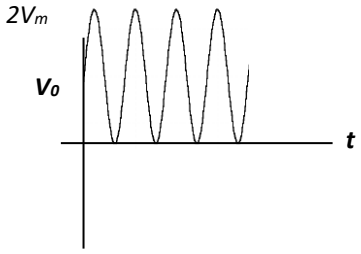


Figure:8 (b) Output waveform.

V. <u>Positive Clamping with Negative Reference Voltage</u>.

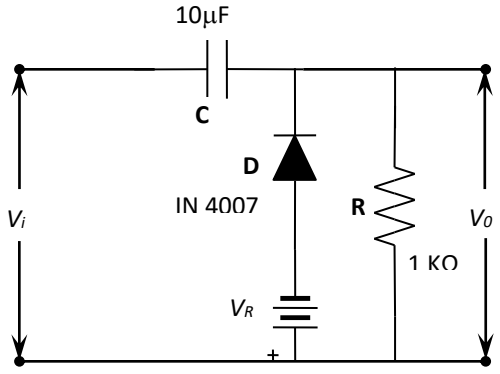


Figure: 9

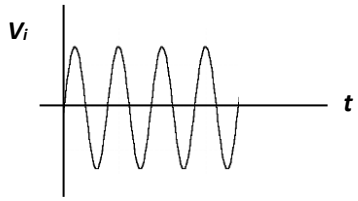


Figure:9 (a).Input waveform

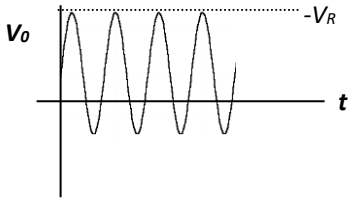


Figure:9(b) Output waveform.

VI. <u>Positive Clamping with Positive reference Voltage.</u>

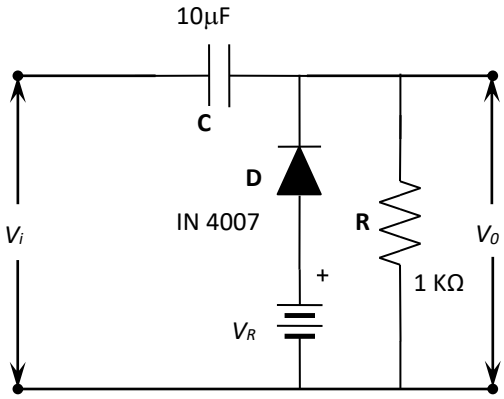


Figure: 10

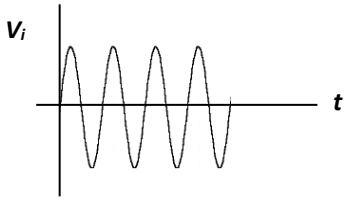


Figure:10 (a).Input waveform

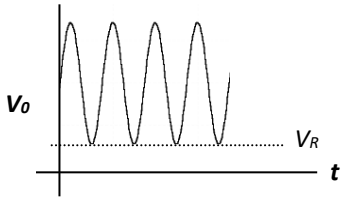


Figure:10 (b) Output waveform

OBSERVATION TABLE:

S.No	Type of Clamping	Vin	V_{ref}	Theoretical Calculation Vout=Vin±Vm	Practical Calculation
1					
2					

PROCEDURE:

1. Connect the circuit as shown in the figure 3.
2. Connect the function generator at the input terminals and CRO at the output terminals of the circuit.
3. Apply a sine wave greater than the reference voltage, and signal of frequency 1kHz at the input and observe the output waveforms of the circuits in CRO.

CONCLUSION:

Conclusion can be made on theoretical and practical values of cutin voltages of diode and also conclude on theoretical and practical output wave forms for different reference voltages

.DESIGN PROBLEMS:

1. Design a positive peak clamper with the V_R=2V
2. Design a negative peak clamper with the V_R=2V
3. Design a positive peak clamper with the R=1K and V_R=3V
4. Design a negative peak clamper with the R=1K and V_R=2V
5. Design a positive bias peak clamper with the V_R=2V
6. Design a positive peak clamper with the V_R= -2V
7. Design a negative peak clamper with the V_R=2V
8. Design a positive peak clipper with Germanium diode.
9. Design a positive peak clipper with the V_R=2V
10. Design a negative peak clamper for R_1= 100K and C=0.01µF with V_R= -2V
11. Design a positive peak clipper with the V_R=2V
12. Design a negative peak clipper with the V_R=2V

13. Design a positive peak clipper with the R=1K and V_R=3V
14. Design a negative peak clipper with the R=1K and V_R=2V
15. Design a positive bias peak clipper with the V_R=2V
16. Design a positive peak clipper with the V_R= -2V
17. Design a negative peak clipper with the V_R=2V
18. Design a slicer with the V_{R1}=2V and V_{R2}=5V
19. Design a slicer with the V_{R1}=8V and V_{R2}= -5V
20. Design a positive peak clipper with Germanium diode.
21. Design a positive peak clipper with the V_R=2V
22. Design a positive bias peak clamper with the V_R=2V
23. Design a positive peak clamper with the V_R= -2V
24. Design a negative peak clamper with the V_R=2V
25. Design a positive peak clipper with Germanium diode
26. Design a negative peak clamper for R_1= 100K and C=0.01µF with V_R= -2V
27. Design a positive peak clipper with the V_R=2V
28. Design a negative peak clipper with the V_R=2V
29. Design a slicer with the V_{R1}=8V and V_{R2}= -5V
30. Design a positive peak clipper with Germanium diode

VIVA QUESTIONS:

1. What are the applications of clamping circuits?
2. What is the synchronized clamping?
3. Explain the Principle of operation of Clampers.
4. What is clamping circuit theorem.
5. What is the function of capacitor in clamper circuit?
6. What are the effects of diode characteristics on the output of the Clamper?
7. If we interchange the diode and the capacitor in fig 1 above, how the circuit behaves?
8. What is floating output and grounded output for a DC power supply? If we use grounded output PS in the above circuits, what will happen?
9. Calculate the power dissipation in the Resistor for any one of the above circuits?
10. What is the difference between a clipper and a clamper?
11. 1. Explain the operation of a clamping circuit for a square wave input?
12. Differentiate the clippers with clampers?
13. Give the applications of clampers?
14. What are the applications of clamping circuits?
15. What is the synchronized clamping?
16. What is a clamper?

17. Explain the Principle of operation of Clampers?

18. What is clamping circuit theorem.

19. What is the function of capacitor in clamper circuit?

20. What are the effects of diode characteristics on the output of the Clamper?

21. If we interchange the diode and the capacitor in fig 1 above, how the circuit behaves?

22. Calculate the power dissipation in the Resistor for any one of the above circuits?

23. What is the difference between a clipper and a clamper?

24. . What are the other names for clampers?

25. Give some practical applications of clamper?

26. What is the purpose of shunt resistance in clamper?

27. What is used for clamper?

28. What is parpuse of clampers?

29. What is mean by clamper?

30. Explain the principle of operation of clampers.

EXPT NO: 9

TRANSISTOR AS A SWITCH

AIM:

Design Transistor to act as a Switch and verify the operation. Choose V_{CC} = 10V, I_{Cmax} = 10 mA, h_{fe} = 50, V_{CESat} = 0.2, V_{in} = 4Vp-p, V_{BESat}= 0.6 V

APPARATUS:

1. Transistor (BC 107).
2. Breadboard.
3. CRO.
4. Resistors (1KΩ, 8.2KΩ).
5. DC power supply.
6. Function Generator.
7. Connecting patch cards.

THEORY:

When the I/P voltage V_i is negative or zero, transistor is cut-off and no current flows through $R_c$hence $V_0 \cong V_{CC}$ when I/P Voltage V_i jumps to positive voltage, transistor will be driven into saturation. Then

$$V_0 = V_{cc} - I_C R_C \cong V_{CESat}$$

DESIGN PROCEDURE:

When Q is ON $R_C = \frac{V_{CC} - V_{CESat}}{I_{C\max}}$

$= (10\text{-}0.2) / 10 \text{ mA} \quad = 1K\Omega$

$I_B \geq I_{Cmax} / h_{fe}$

$\geq 10mA / 50$

$I_B \quad \geq 0.2$ mA

To keep transistor remain in ON, I_B should be greater than

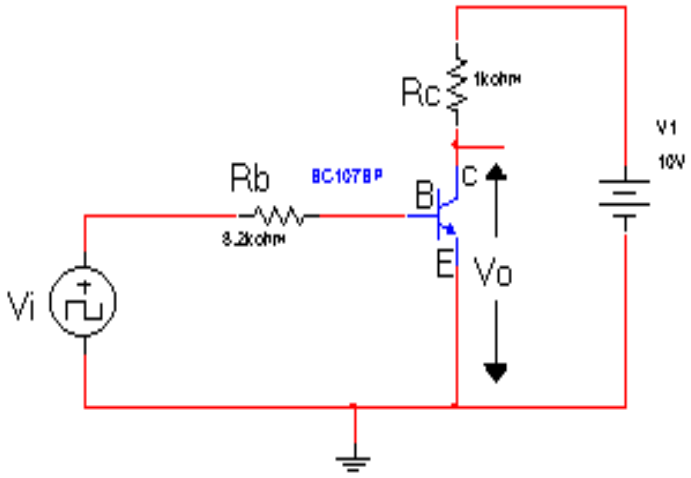
$I_{bmin} = 0.2mA$

$V_{in} = I_B R_B + V_{BE\ Sat}$

$2V = 0.2 \text{ mA } R_B + 0.6V$

$R_B = 7$ K (choose practical values as 8.2 K)

CIRCUIT DIAGRAM:



OBSERVATION TABLE:

S.No	Input Voltage From RPS	Transistor Action	Theoretical Calculation Ib.Ic,Vce-output	Practical Calculation
1				
2				

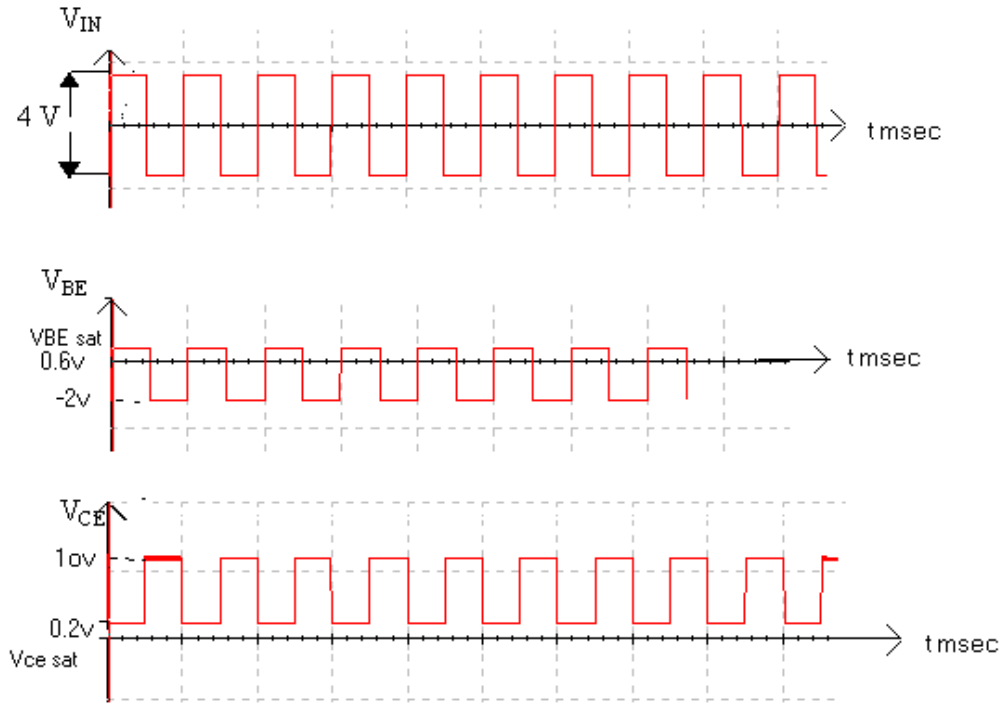
PROCEDURE:

1. Connect the circuit as shown in figure.
2. Apply the Square wave 4 Vp-p frequency of 1 KHz
3. Observe the waveforms at Collector and Base and plot it.

PRECAUTIONS:

1. When you are measuring O/P waveform at collector and base, keep the CRO in DC mode.
2. When you are measuring $V_{BE\ Sat}$, $V_{CE\ Sat}$ keep volts/div switch at either 0.2 or 0.5 position.
3. When you are applying the square wave see that there is no DC voltage in that. This can be checked by CRO in either AC or DC mode, there should not be any jumps/distortion in waveform on the screen.

EXPECTED WAVEFORMS:



RESULT:

Transistor as a switch has been designed and O/P waveforms are observed.

DESIGN PROBLEMS:

1. Design a transistor as switch for Vcc=15 V, Ic(max)=5mA, h_{fe}=20, Vce(sat)=0.3V, Vin= 4Vpp
2. Design a transistor as switch for Vcc=10 V, Ic(max)=3mA, h_{fe}=18,Vce(sat)=0.3V, Vin= 5Vpp
3. Design a transistor as switch for Vcc=12 V, Ic(max)=7mA, h_{fe}=15, Vce(sat)=0.3V, Vin= 6Vpp
4. Design a transistor as switch for Vcc=9V, Ic(max)=6.5mA, h_{fe}=50, Vce(sat)=0.3V, Vin= 3Vpp
5. Design a transistor as switch for Vcc=5 V, Ic(max)=5mA, h_{fe}=20, Vce(sat)=0.3V, Vin= 4Vpp
6. Design a transistor as switch for Vcc=5 V, C=1µF ,R_1=R_2=1K , R_E=5K with BC107
7. Design a transistor as switch for Vcc=12 V, C=10µF ,R_1=R_2=1K , R_E=5K with BC107
8. Design a transistor as switch for Vcc=10 V, C=100µF ,R_1=R_2=1K , R_E=5K with BC107
9. Design a transistor as switch for Vcc=10V, C=4.7µF ,R_1=R_2=1K , R_E=5K with BFW10

10. Design a transistor as switch for Vcc=12 V, C=10μF ,R_1=R_2=1K , R_E=5K with BFW10

VIVA QUESTIONS:

1. Differentiate Diode and Transistor as a switch?
2. Mention typical values of V_{BE} Sat, V_{CE} Sat for both Si, Ge Transistors?
3. Define ON time and OFF time of the transistor?
4. In which regions Transistor acts as a
5. Explain phenomenon of "latching "in a Transistor switch?
6. Define Rise time & fall time of a transistor switch?
7. Define Storage time?
8. Define delay time?
9. What is the phase difference between the input waveform and the output waveform, when the transistor is conducting?
10. What modifications are to be done in the above circuit if we use PNP transistor instead of NPN transistor?
11. Differentiate Diode and Transistor as a switch?
12. Mention typical values of V_{BE} Sat, V_{CE} Sat for both Si, Ge Transistors?
13. Define ON time and OFF time of the transistor?
14. In which regions Transistor acts as a switch?
15. Explain phenomenon of "latching "in a Transistor switch?
16. Define Rise time & fall time of a transistor switch?
17. Define Storage time?
18. Define delay time?
19. What is the phase difference between the input waveform and the output waveform, when the transistor is conducting?
20. What modifications are to be done in the above circuit if we use PNP transistor instead of NPN transistor?
21. What are the limitions of transistor switch?
22. What is the turn on time of a transistor?
23. Define the transistor?
24. Explain about the transistor?
25. 1) What is transistor? what are the types of transistors?
26. Define n-type and p-type semiconductors?

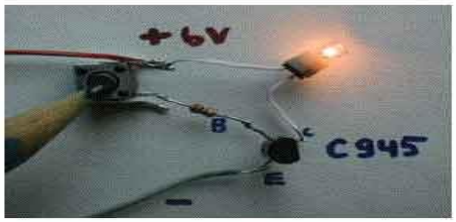
27. What is doping?
28. What are three basic transistor connection modes?
29. Which mode is most preferred? Why?
30. Define current amplification factor of a transistor?

REAL TIME APPLICATIONS OF BIPOLAR JUNCTION TRANSISTOR:

There are two types of **applications of bipolar junction transistor**, switching and amplification.

Transistor as a Switch

For switching applications transistor is biased to operate in the saturation or cutoff region. Transistor in cutoff region will act as an open switching whereas in saturation will act as a closed switch.



EXPT NO: 10

STUDY OF LOGIC GATES AND SOME APPLICATIONS

Prior to the Lab session:

1. Study about digital logic gates, symbols and truth tables.
2. Study about universal logic gates and realization of basic gates using universal gates.
3. Study the procedure for conducting the experiment in the lab.

Objectives:

1. Study of logic gates using IC's.
2. Realization of basic gates using NAND & NOR gates (Universal gates).
3. Implementation of Half Adder and Full Adder using logic gate.

Apparatus:

1. IC 7400, IC 7404, IC 7408, IC 7432, IC 7486 - 1No. each
2. Connecting patch chords
3. IC Trainer Kit.

Theory:

A logic gate performs a logical operation on one or more logic inputs and produces a single logic output. The logic is normally performed as Boolean logic and is most commonly found in digital circuits.

The different types of logic gates are:

i. NOT gate
ii. OR gate
iii. AND gate
iv. EX-OR gate
v. NAND gate
vi. NOR gate

Inverter or NOT gate:

The inverter is a logic gate which has only one input & one output. In inverter a low input produces a high output and a high input produces a low output.

Logic equation is: $Y = \overline{A}$ Digital IC for NOT: **IC 7404.**

AND gate:

AND gate is a logic gate Which can have two or more inputs. But there is only one output. The output of AND gate is high only if all inputs are high. Even if one input is low, the output will be low.

Logic equation is: **Y = AB** Digital IC for AND: **IC 7408.**

OR gate:

An OR gate is a logic gate Which can have two or more inputs and a single output. The output of an OR gate is high if any of the inputs or all inputs are high. The output is low only if all the inputs are low.

Logic equation is: **Y= A + B** Digital IC for OR: **IC 7432.**

NAND gate:

NAND gate is a combination of AND & NOT gates. Thus NAND gate is the inverse of AND gate. The output is low when all inputs are high. The output is high for all the remaining combinations.

Logic equation is: $Y = \overline{AB}$ Digital IC for NAND: **IC 7400.**

NOR gate:

NOR gate is a combination of OR & NOT gates. Thus NOR gate is the inverse of OR gate. When all or either of the inputs are high output is low. The output of NOR gate is high only when all inputs are low.

Logic equation is: $Y = \overline{A + B}$ Digital IC for NOR: **IC 7402.**

EX-OR gate:

In EX-OR gate if either of the inputs is high, output will be high. If both the inputs are high output will be low. If both inputs are low then also output will be low.

Logic equation is: $Y = A\overline{B} + B\overline{A} = A \bigoplus B$ Digital IC for EX-OR: **IC 7486.**

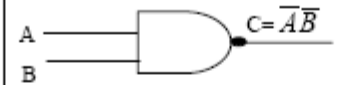
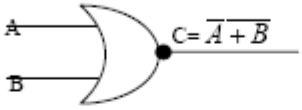
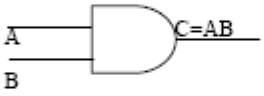
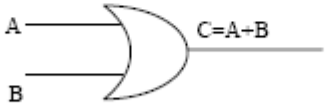
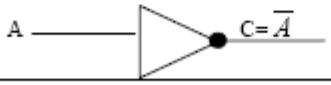
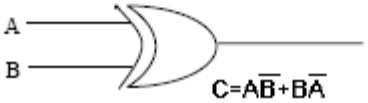
S.NO	GATE	SYMBOL	INPUTS		OUTPUT
			A	B	C
1.	NAND IC 7400		0	0	1
			0	1	1
			1	0	1
			1	1	0
2.	NOR IC 7402		0	0	1
			0	1	0
			1	0	0
			1	1	0
3.	AND IC 7408		0	0	0
			0	1	0
			1	0	0
			1	1	1
4.	OR IC 7432		0	0	0
			0	1	1
			1	0	1
			1	1	1
5.	NOT IC 7404		1	-	0
			0	-	1
6.	EX-OR IC 7486		0	0	0
			0	1	1
			1	0	1
			1	1	0

Table. 5.1 Logic gates symbols and truth tables

Circuit diagrams:

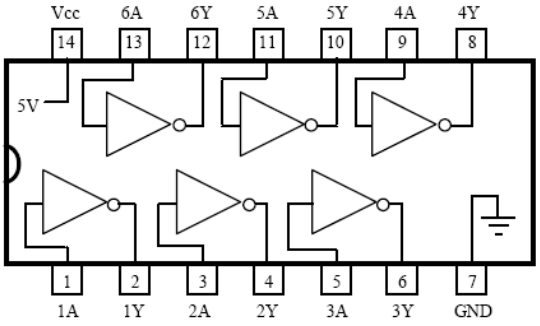


Fig 5.1 NOT gate (IC 7404)

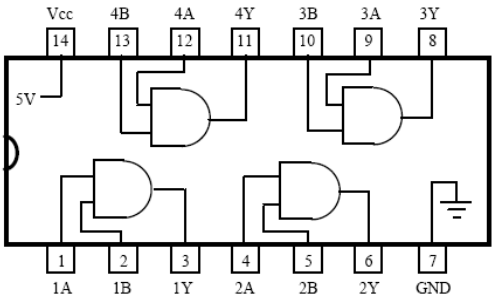


Fig 5.2 AND gate (IC 7408)

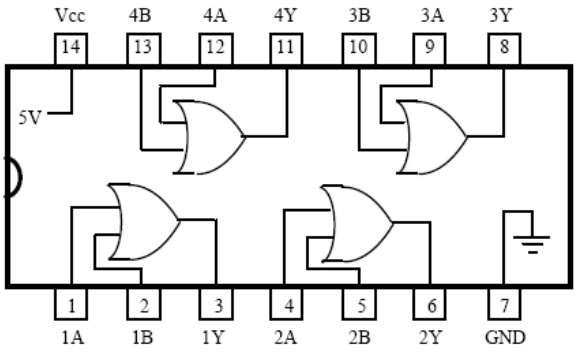


Fig 5.4 OR gate (IC 7432)

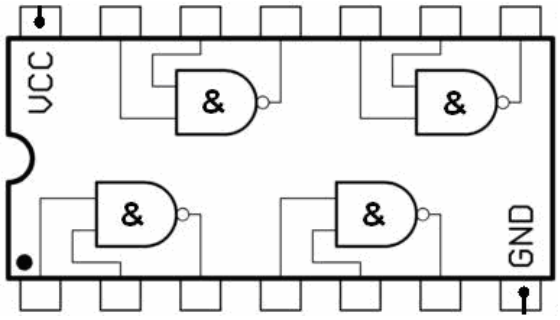


Fig 5.5 NAND gate (IC 7400)

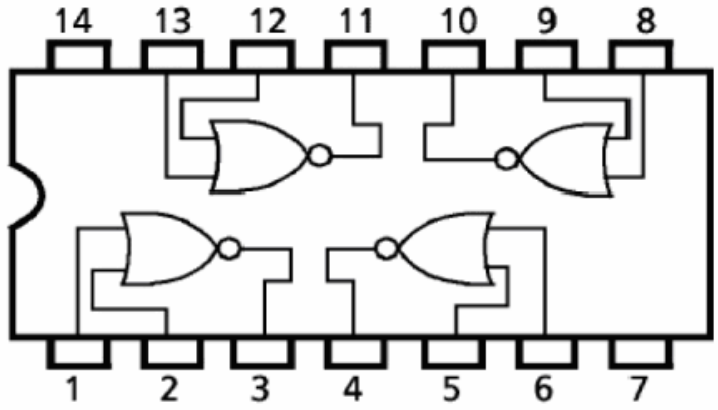
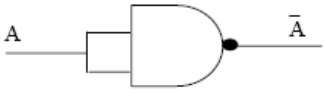


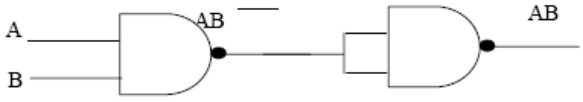
Fig 5.6 NOR gate (IC 7402)

Realization of basic gates using NAND gates:

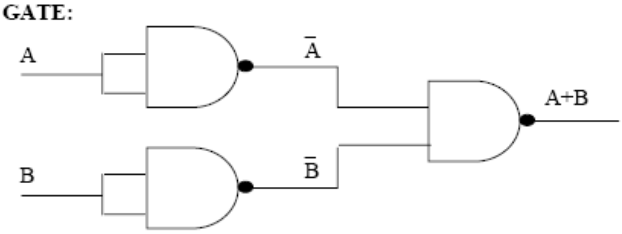
NOT GATE:



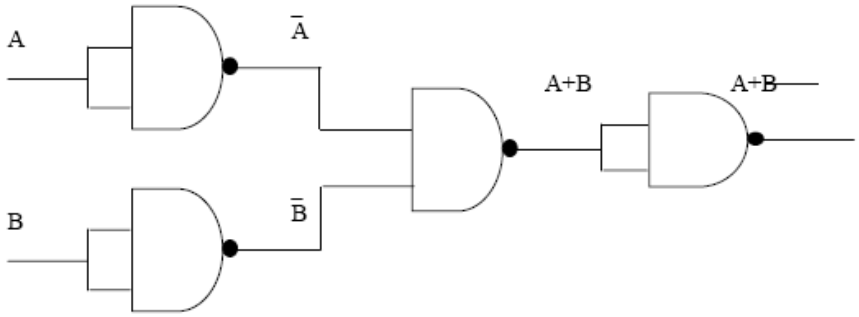
AND GATE:



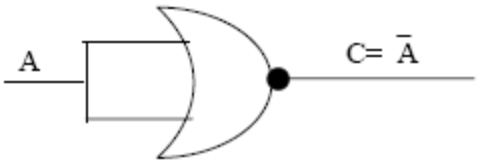
OR GATE:



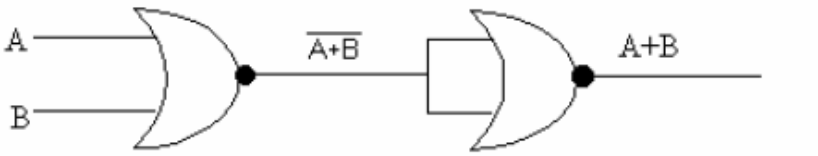
NOR GATE:



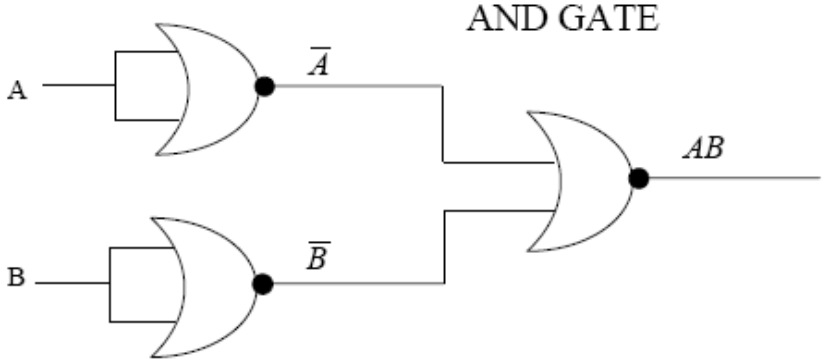
NOT GATE



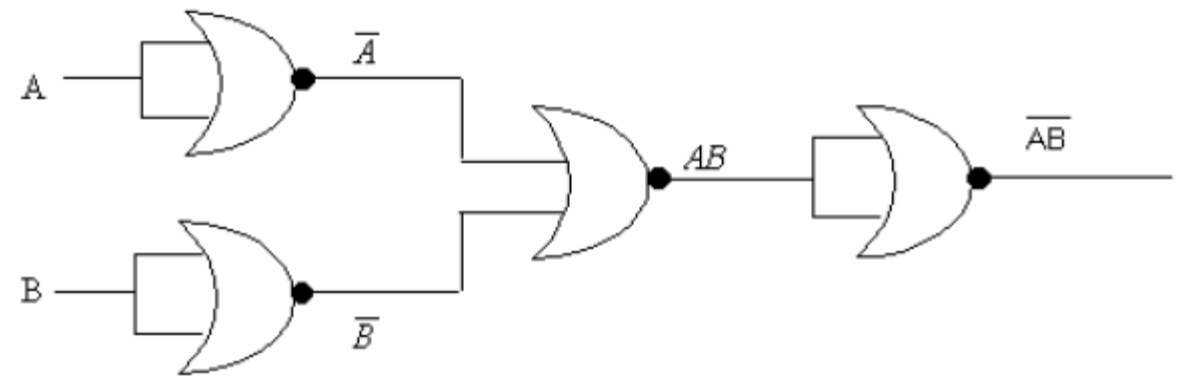
OR GATE



AND GATE



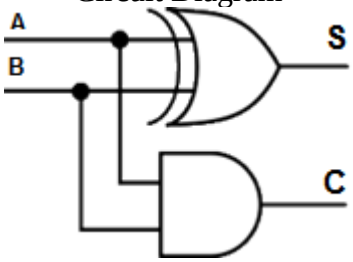
NAND GATE



Implementation of Half Adder and Full Adder using logic gates:

Half Adder:

Circuit Diagram

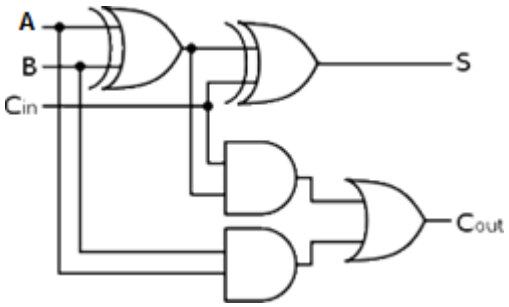


Truth Table

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full Adder:

Circuit Diagram



Truth Table

A	B	C_i	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Procedure:

1. Connect the NOT gate using digital IC's as shown in the figure 5.1.
2. Use +5V for logic 1 and 0V for logic 0.
3. Feed the logic signals 0 or 1 from the logic input switches at the inputs A & B.
4. Monitor the output using LED indicators and verify its truth table.

5. Repeat step l to 4 for all the remaining gates.

Inference: Truth tables of all logic gates are verified.

Viva Questions:

1. Why NAND & NOR gates are called universal gates?
2. Realize the EXOR gate using minimum number of NAND gates.
3. Give the truth table for EX-NOR (EX-OR+NOT) and realize using NAND gates.
4. Explain the operation of NAND gate when realized using discrete components.
5. What are the logic low and High levels of TTL IC's and CMOS IC's.
6. Compare TTL logic family with CMOS family.
7. Which logic family is called fastest and which logic family is called low power dissipated.
8. Explain the operation of OR, NOR gates when realized using discrete Components.
9. Why the transistor operates as NOT gate.
10. What is fan-in and fan-out?
11. Why this IC series starts with 74XX.

EXPT NO: 11

STUDY OF FLIP FLOPS AND SOME APPLICATIONS

Objective: To realize and implement

- Set-Reset (SR) latch using NOR gates (active high circuit).
- SR, JK, D, and T Flip-Flops using IC's and breadboard.

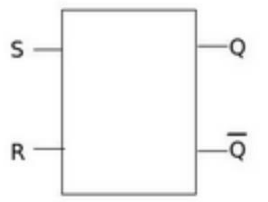
Components Required:

- Mini Digital Training and Digital Electronic Sets.
- IC 7404, IC 7408, IC 7411, IC 7474, IC 7476.

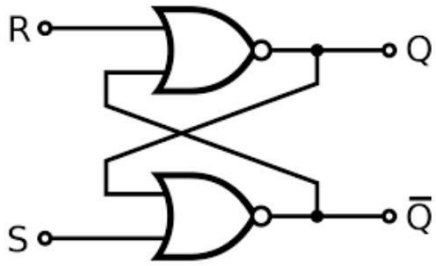
Theory:

Logic circuits for digital systems are either combinational or sequential. The output of combinational circuits depends only on the current inputs. In contrast, sequential circuit depends not only on the current value of the input but also upon the internal state of the circuit. Basic building blocks (memory elements) of a sequential circuit are the flip-flops (FFs). The FFs change their output state depending upon inputs at certain interval of time synchronized with some clock pulse applied to it. Usually any flip-flop has normal inputs, **present state** Q(t) as circuit inputs and two outputs; **next state** Q(t+1) and its complementary value; Q`. We shall discuss most widely used latches that are listed below.

1. **SR flip-flop:**



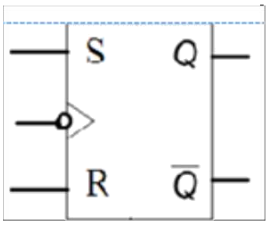
Symbol of SR latch



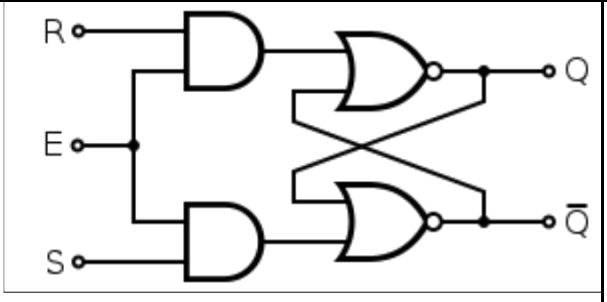
Logic diagram of SR FF
NOR Implementation (Active high)

S	R	Q(t+1)	Comment
0	0	Q(t)	NC
0	1	0	Reset
1	0	1	Set
1	1	X	undefined

Characteristic Table



Symbol of Clocked SR FF



SR flip-flop with Enable line

E	S	R	Q(t+1)	Comment
0	X	X	Q(t)	NC
1	0	0	Q(t)	NC
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	X	undefined

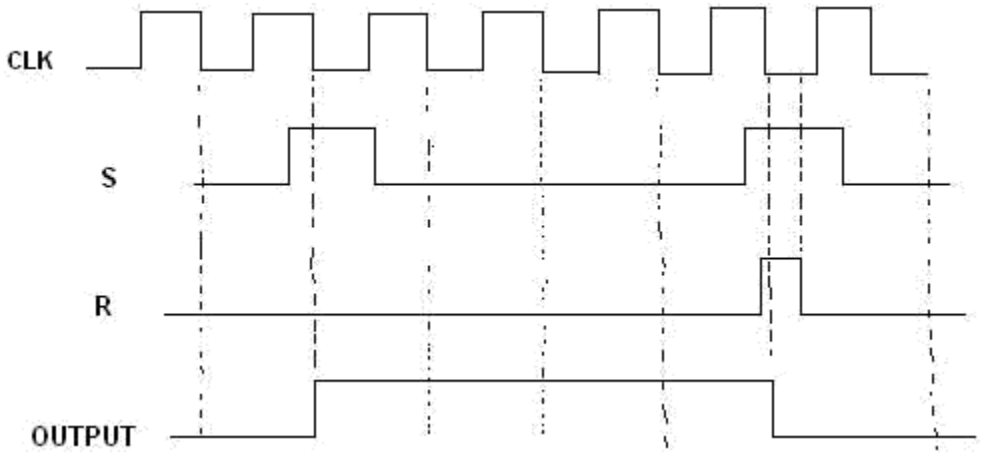
Characteristic Table

	00	01	11	10
0			x	1
1	1		x	1

Q(t+1)=S+R`Q(t)

Edge triggered flip-flop:

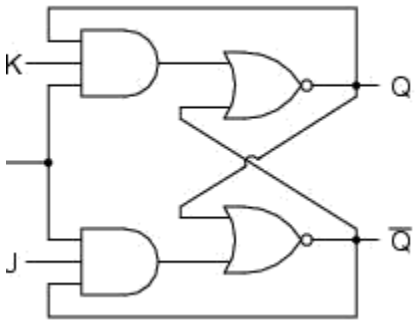
The edge-triggered FF means: on the rising or falling edge of the clock, the output Q(t+1) is computed given the value of the inputs (S and R) at that moment and the previous output Q(t). The output can be only changed at the clock edge, and if the input changes at other times, the output will be unaffected.



Timing diagram of clocked SR flip-flop

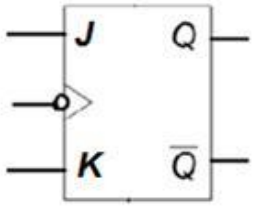
2. JK flip-flop:

The JK flip-flop is the modified version of SR flip-flop with no invalid state; i.e. the state J=K=1 is not forbidden. It works such that J serves as set input and K serves as reset. The only difference is that for the combination J=K=1 this flip-flop; now performs an action: it inverts its state.



Logic diagram of JK FF from SR FF

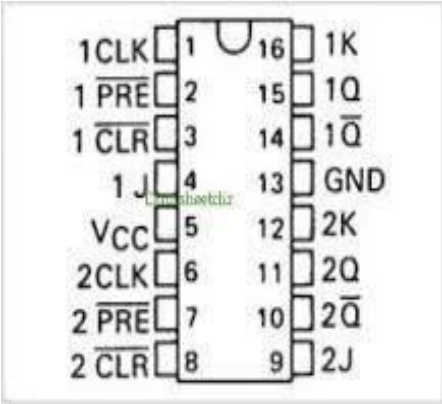
R=KQ(t)
S=JQ`(t)
Q(t+1)=S+R`Q(t)
= JQ`(t)+(KQ(t))`Q(t)
= JQ`(t)+K`Q(t)
Characteristic equation



Symbol of JK FF

CLK	J	K	Q(t+1)	comment
0	X	X	Q(t)	NC
1	0	0	Q(t)	NC
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	Q`(t)	Toggle

Characteristic Table



Pin diagram of IC 7476

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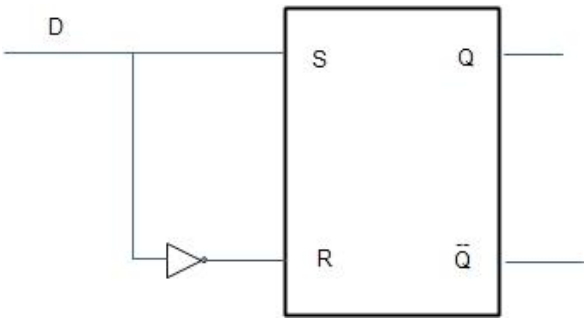
3. D- FLIP FLOP:



D flip flop Truth table

CLK	D	Q
0	*	Last State
1	0	0
1	1	1

D Flip Flop Characteristic Table

D	Q_t	Q_{t+1}
0	0	0
0	1	0
1	0	1
1	1	1

4. T-FLIP FLOP

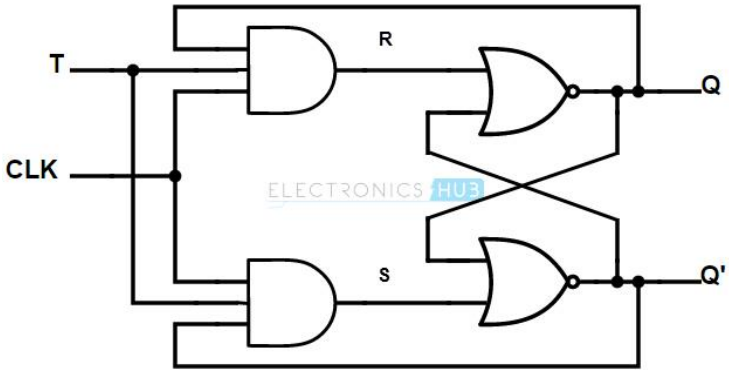


fig: CIRCUIT DIAGRAM

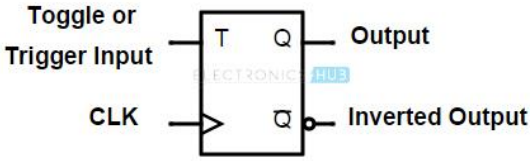


Fig: SYMBOUL

	Previous		Next	
T	Q_{Prev}	Q'_{Prev}	Q_{Next}	Q'_{Next}
0	0	1	0	1
0	1	0	1	0
1	0	1	1	0
1	1	0	0	1

Fig: T-flip flop truth table

Procedure:

1. Implement active high SR flip flop using IC's and breadboard and verify the truth table.
2. Implement D, JK and T Flip-Flops using IC's and breadboard and verify the truth table.

Conclusions: Basic memory elements are implemented and verified.

EXPT NO: 12

MONOSTABLE AND A STABLE MULTIVIBRATORS

AIM :

To design a monostablemultivibrator to generate clock pulse for a given frequency and obtain the waveforms and test its performance

COMPONENTS REQUIRED:

1. Resistors		
2. Capacitors.		
3. Transistors	2N2369	2 No.s

APPARATUS REQUIRED:

1. CRO	1Hz-20MHz	1 No.
2. Power supply	0-30V	1 No.
3. Bread board		
4. Connecting wires		

CIRCUIT DIAGRAM:

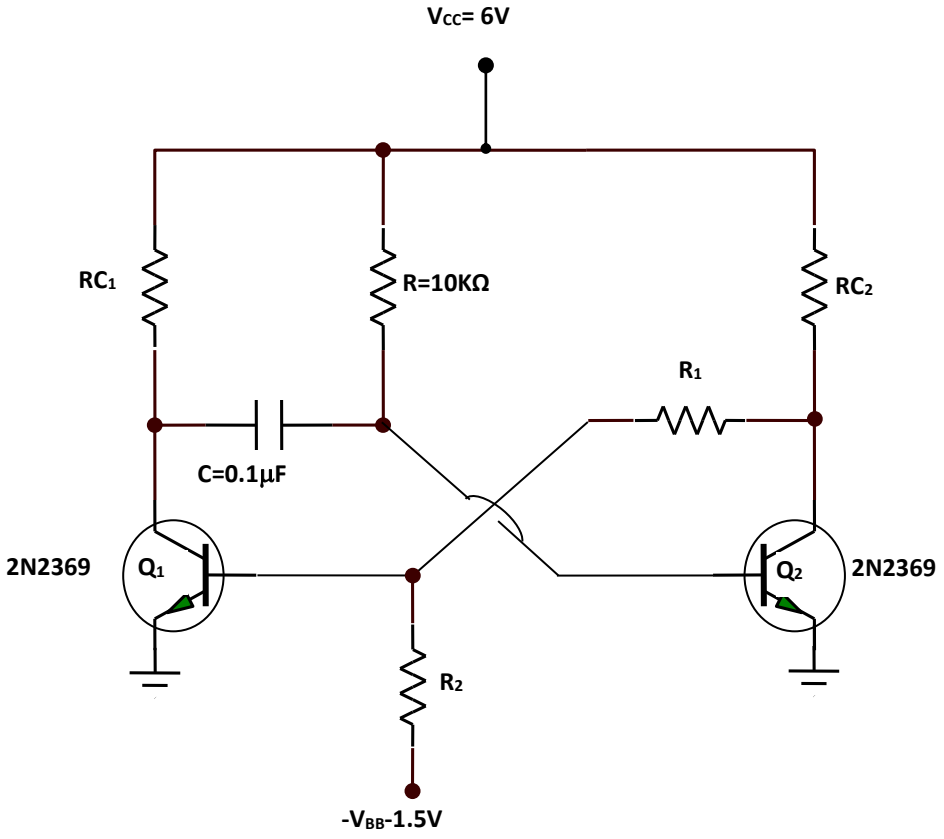


Figure-1

THEORY :

A monostable multivibrator has only one stable state, the other state being quasi-stable. Normally the multivibrator is in the stable state, and when an external triggering pulse is applied, it switches from the stable to the quasi-stable state. It remains in the quasi-stable state fro a short duration, but automatically reverts i.e. switches back to its original stable state, without any triggering pulse'.

Principle of operation

A collector-coupled Monostable multivibrator of the two transistors Q_1 and Q_2, Q_1 is normally OFF and Q_2 is Normally ON. Resistor R_1 and R_2 are connected to the normally OFF transistor, and the capacitor C is connected to the normally ON transistor.

It is seen from the circuit of the monostable multivibrator that, under normal conditions, the supply voltage V_{CC} provides enough base drive to the transistor Q_2 through resistor R, with the result that Q_2 goes into saturation. With Q_2 ON, Q_1 goes OFF, as already studied in the context of binary operation.

With Q_2 ON and Q_1 OFF, the capacitor finds a charging path. The voltage across the capacitor is V_{CC} with polarity. It is obvious that in the stable state of the multivibrator, Q_2 is ON and Q_1 is OFF.

If the negative triggering pulse is applied to the collector of Q_1, it is transmitted to the base of Q_2 through the capacitor, and hence makes the base of Q_2 negative. Immediately Q_2 goes OFF and Q_1 becomes ON. However, this is only a quasi-stable state as is obvious form the following observation.

With Q_1 ON and Q_2 OFF, the capacitor C finds a discharging path. As the capacitor discharges, it is seen that the potential at the base of the transistor Q_2 becomes less and less negative, and after a time, we have $V_B = V_\gamma$, the cut-in-voltage of Q_2.

As soon as V_B crosses the level of V_γ, Q_2 starts conducting and gets saturated. When Q_2 becomes ON, Q_1 becomes OFF. Thus the original stable state of the multivibrator is restored.

[In quasi-stable state: Q_1 is ON and Q_2 is OFF]

The interval during which the quasi-stable state of the multivibrator persists i.e., Q_2 remains OFF is dependent upon the rate at which the capacitor C discharges. This duration of the quasi-stable state is termed as delay time or pulse width or gate time. It is denoted as T. The wave forms of the voltage at base of the transistor Q_2 and C (Collector of Q_1)

Design:

V_{CE} = 5.56v, V_{CC} = 6v, $V_{CE(sat)}$ = 0.3v, $V_{BE(sat)}$, = 0.7v, I_C = 6mA,V_F= -0.3v

Rc = (V_{CC}–$V_{CE(sat)}$)/I_C.

$$V_F = \frac{-V_{BB}R_1}{R_1+R_2} + \frac{V_{CE(sat)}R_2}{R_1+R_2}$$

$$V_{CE} = \frac{V_{CC}R_1}{R_1+R_C} + \frac{V_{BE(sat)}R_C}{R_1+R_C}$$

Find the values of R_1 and R_2

Theoretical gate width 'T' with Q_1 in saturation = 0.69RC

Observation Table:

S.No	Theoretical Time Period ($T = T_{ON}$) =0.69RC Calculation	Practical Time Period ($T = T_{ON}$) Calculation
1		

\

PROCEDURE:

1. Connect the circuit as shown in figure.
2. With the help of a triggering circuit and using the condition T (trig) > T(Quasi) a pulse waveform is generated.
3. The output of the triggering circuit is connected to the base of the off transistor.
4. The Off transistor goes into ON state.
5. Observe the waveforms at V_{BE1}, V_{BE2}, V_{CE1}, V_{CE2}
6. Keep the DC- AC control of the Oscilloscope in DC mode.
7. Compare the theoretical and practical gate widths.

EXPECTED WAVEFORMS:

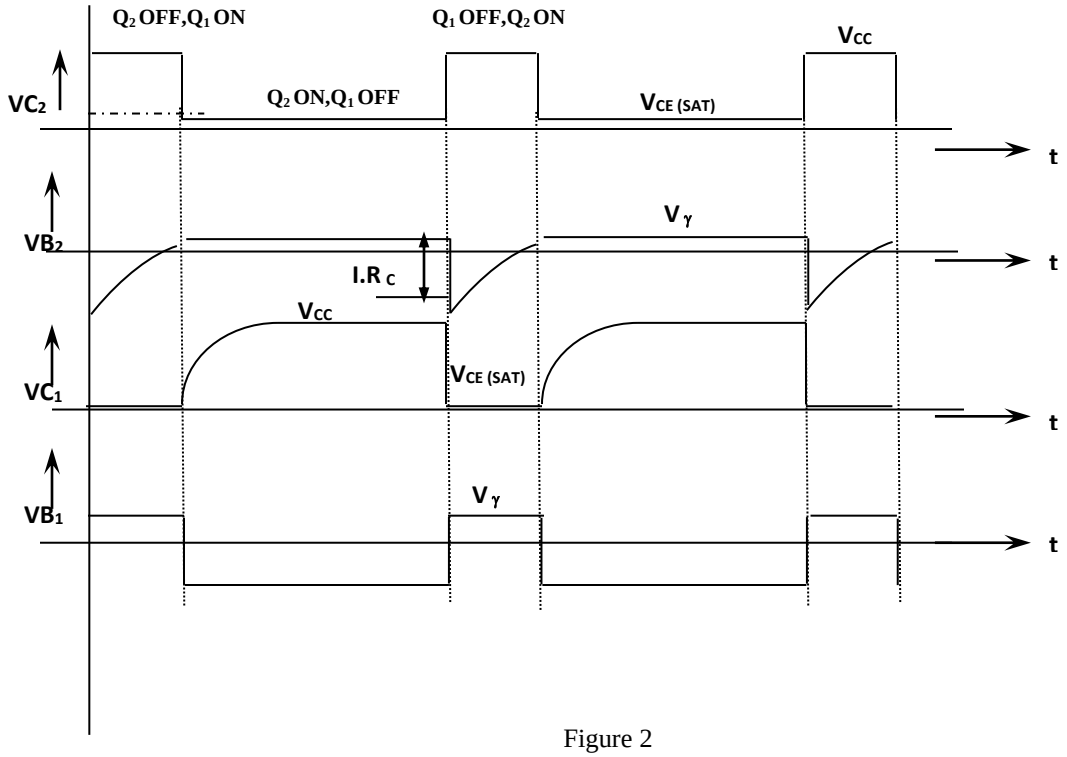


Figure 2

Observations:

T_{ON} (Theoretical) = 0.69RC =
T_{ON} (practical) =

CONCLUSION:

Conclusion can be made on time gate width 'T' of the monostablemultivibrator theoretically and practically and output waveforms of the multi vibrator are identical or not when compared with the theoretical wave forms

A STABLE MULTIVIBRATOR

AIM :

To design an Astable Multivibrator to generate clock pulse for a give frequency and obtain the wave forms and test its performance.

COMPONENTS REQUIRED:

1. Resistors		
2. Capacitors	0.1 μf	2 No.s
3. Transistors	2N2369	2 No.s

APPARATUS:

1. CRO	1Hz-20MHz	1No.
2. Power supply	0-30V	1 No
3. Bread board		
4. Connecting wires		

THEORY:

An Astablemultivibrator has two quasi-stable states, and it keeps on switching between these two states, by itself, No external triggering signal is needed. The astablemultivibrator cannot remain indefinitely in any of these two states. The two amplifiers of an astablemultivibrator are regeneratively cross-coupled by capacitor.

Principle:

A collector-coupled astablemultivibrator using n-p-n transistor in figure 1. The working of an astablemultivibrator can be studied with respect to the figure1.

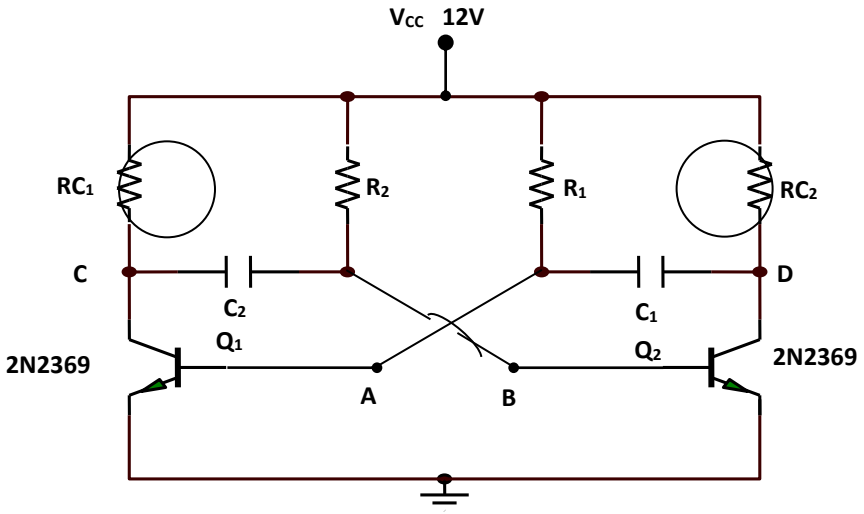


Figure:1

Let it be assumed that the multivibrator is already in action and is oscillating i.e., switching between the two states. Let it be further assumed that at the instant considered, **Q_2 is ON and Q_1 is OFF**.

i) Since Q_2 is ON, capacitor C_2 charges through resistor R_{C1}. The voltage across C_2 is V_{CC}.

ii) Capacitor C_1discharges through resistor R_1, the voltage across C_1 when it is about to start discharging is V_{CC}.(Capacitor C_1 gets charged to V_{CC} when Q_1 is ON).

As capacitor C_1 discharges more and more, the potential of point A becomes more and more positive (or less and less negative), and eventually V_A becomes equal to V_γ, the cut in voltage of Q_1. For $V_A > V_\gamma$, transistor Q_1 starts conducting. When Q_1 is ON Q_2 becomes OFF.

Similar operations repeat when Q_1 becomes ON and Q_2 becomes OFF.

Thus with **Q_1 ON** and **Q_2 OFF,** capacitor C_1 charges through resistor R_{C2} and capacitor C_2 discharges through resistor R_2. As capacitor C_2 discharges more and more , it is seen that the potential of point B becomes less and less negative (or more and more positive), and eventually V_B becomes equal to V_γ, the cut in voltage of Q_2. when $V_B > V_\gamma$, transistor Q_2 starts conducting. When Q_2 becomes On, Q_1 becomes OFF.

It is thus seen that the circuit keeps on switching continuously between the two quasi-stable states and once in operation, no external triggering is needed. Square wave voltage are generated at the collector terminals of Q_1 and Q_2 i.e., at points C and D.

Design:

I_C max = 5 mA ; V_{CC} = 12 V; $V_{CE\,(SAT)}$ = 0.2V

$R_C = (V_{CC} - V_{CE(SAT)}) \;/\; I_{C\,MAX}$

Let C = 0.1 μf and R= 10KΩ

$T = 0.69\,(R_1C_1+R_2C_2) = 0.69(2RC)$ $\quad \because \quad (R_1=R_2 \;;\; C_1=C_2)$

$=T_{ON}+T_{OFF}$

OBSERVATION TABLE:

S. No	Theoretical Time Period ($T(T_{ON} + T_{OFF})$) = 1.38RC Calculation	Practical Time Period($T = T_{ON} + T_{OFF}$)) Calculation
1		

PROCEDURE:

1. Connect the circuit as shown in figure 1.
2. Observe the waveforms at V_{BE1}, V_{BE2}, V_{CE1}, V_{CE2} and find frequency.
3. Vary C from 0.01 to 0.001μF and measure the frequency at each step.
4. Keep the DC- AC control of the Oscilloscope in DC mode.

EXPECTED WAVEFORMS:

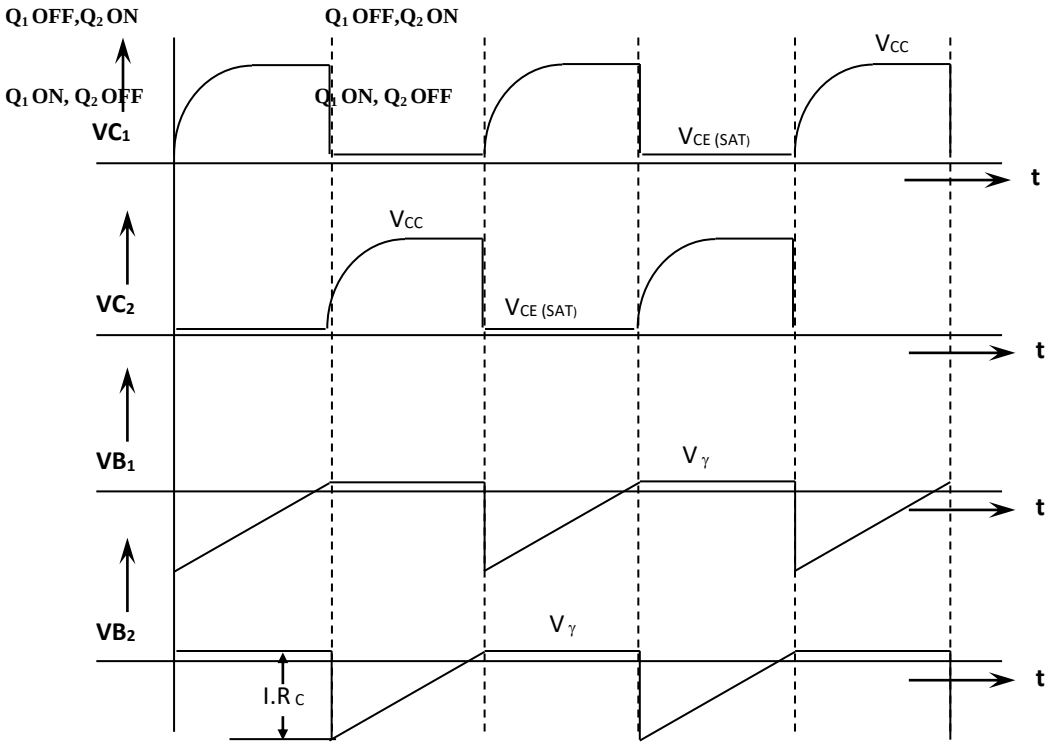


Figure 2

Observations:

T_{ON} (Theoritical) = 0.69RC = **T_{OFF} (Theoritical)** = 0.69RC =
$T(T_{ON} + T_{OFF})$ (Theoritical) = **1.38**RC =
T_{ON} (practical) = **T_{OFF} (practical)** = **$T(T_{ON} + T_{OFF})$ (practical)** =

CONCLUSION:

Conclusion can be made on time period of the output waveforms of the Astable multivibrator theoretically and practically and output waveforms of the multi vibrator are identical or not WHEN compared with the theoretical wave forms.

DESIGN PROBLEMS:

1. Design a Monostablemultivibrator with Vcc=10V, R_1=2K, R_2=20K, Rc_1=Rc_2 =2K, C=0.1µF, For the pulse width of 1µsec
2. Design a One-shot multivibrator with Vcc=12V, R_1=2K, R_2=20K, Rc_1=Rc_2 =2K, C=0.1µF at Vin=4V
3. Design a Monostablemultivibrator with Vcc=10V, R_1=5K, R_2=20K, Rc_1=Rc_2 =2K, C=0.1µF at Vin=8V
4. Design a Monostablemultivibrator with Vcc=10V, R_1=5K, R_2=25K, Rc_1=Rc_2 =2K, C=10µF, For the pulse width of 1µsec
5. Design a One-shot multivibrator with Vcc=10V, R_1=3K, R_2=25K, Rc_1=Rc_2 =2K, C=10µF at Vin=5V
6. Design a Monostable with BFW10 and R_1=2K, R_2=20K, Rc_1=Rc_2 =2K, C=0.1µF at Vin=8V with triggering circuit having the values of R_T=1k, c_T=1µF
7. Design Monostable with BFW10 and R_1=5K, R_2=20K, Rc_1=Rc_2 =2K, C=0.1µF at Vin=8V
8. Design a One-shot multivibrator with Vcc=10V, R_1=2K, R_2=15K, Rc_1=Rc_2 =4K, C=0.1µF at Vin=10V
9. Design a Monostablemultivibrator with Vcc=10V, R_1=2K, R_2=20K, Rc_1=Rc_2 =2K, C=0.1µF at Vin=8V with commutating capacitors C_1=C_2=1µF
10. Design a One-shot multivibrator with Vcc=10V, R_1=2K, R_2=20K, Rc_1=Rc_2 =2K, C=10µF at Vin=8V with commutating capacitors C_1=C_2=0.1µF

11. Design a Astable multivibrator with Vcc=10V, R_1=2K, R_2=20K, Rc_1=Rc_2 =2K, , C_1=C_2=0.1µF, For the time period of 1µsec
12. Design a Square wave generator withVcc=10V, R_1=5K, R_2=15K, Rc_1=Rc_2 =5K, C_1=C_2=10 µF, For For the time period of 5µsec
13. 3.Design a Astablemultivibrator with Vcc=10V, R_1=2K, R_2=10K, Rc_1=Rc_2 =2K, C_1=C_2=0.1µF, For the time period of 5µsec
14. 4.Design a Square wave generator withVcc=10V, R_1=2K, R_2=20K, Rc_1=Rc_2 =2K, C_1=C_2=4.7 µF, For For the time period of 1µsec
15. 5 .Design a Astablemultivibrator with Vcc=10V, R_1=2K, R_2=20K, Rc_1=Rc_2 =2K, , C_1=C_2=0.1µF, For the time period of 1µsec
16. 6.Design a Square wave generator withVcc=10V, R_1=2K, R_2=20K, Rc_1=Rc_2 =2K, C_1=C_2=4.7 µF, For For the time period of 1µsec

17. 7 .Design a Astablemultivibrator with Vcc=10V, R_1=2K, R_2=20K, Rc_1=Rc_2 =2K, , C_1=C_2=0.1µF, For the time period of 1µsec
18. 8 .Design a Square wave generator withVcc=10V, R_1=5K, R_2=15K, Rc_1=Rc_2 =5K, C_1=C_2=10 µF, For For the time period of 5µsec
19. 9.Design a Astablemultivibrator with Vcc=10V, R_1=2K, R_2=10K, Rc_1=Rc_2 =2K, C_1=C_2=0.1µF, For the time period of 5µsec
20. 10.Design a Square wave generator withVcc=10V, R_1=2K, R_2=20K, Rc_1=Rc_2 =2K, C_1=C_2=4.7 µF, For For the time period of 1µsec

VIVA QUESTIONS:

1. Explain the operation of collector coupled MonostableMultivibrator?
2. Derive the expression for the gate width of a transistor MonostableMultivibrator?
3. Give the application of a MonostableMultivibrator.
4. What are applications of MonostableMultivibrator?
5. Why is a MonostableMultivibrator called a gating circuit?
6. Explain the waveform of VB1?
7. Describe the operation of the capacitor C3 in the circuit?
8. Why is the time period T also called Delay time?
9. Justify, Why Monostable Multivibrator is called one-shot circuit?
10. Why is the –ve voltage given at the base of Q1 transistor?
11. What is the no of quasi & stable states of Monostable Multivibrator?
12. What is a multivibrator? What is a quasi state?
13. What are applications of Monostable Multivibrator?
14. The monostable multivibrator is also called __, ___, __, ___ or ___?
15. A Monostable Multivibrator generates __ waveform?
16. Why is the time period T also called Delay time?
17. Justify, Why Monostable Multivibrator is called one-shot circuit?
18. In monostable multivibrator, the coupling elements are __?
19. What is a switching circuit?
20. What are the other names of monostable multivibrator?
21. What are the applications of monostable multivibrator?
22. What is a switching circuit?
23. Justify that the Astable Multivibrator is a two stage RC coupled Amplifier using negative feedback.
24. What is the difference between a switching transistor and an ordinary transistor?

25. What is the effect of slew rate on the working of an Op-amp Multivibrator?
26. Is it possible to change time period of the waveform with out changing R& C? Support your answer?
27. Collector waveforms are observed with rounded edges. Explain?
28. Explain charging and discharging of capacitors in an AstableMultivibrator?
29. How can an Astable multivibrator be used as VCO?
30. Why do you get overshoots in the Base waveforms?

REAL TIME APPLICATIONS OF MONOSTABLE AND A STABLE MULTIVIBRATORS :

1. Monostable vibrators are used in analog systems to control an output signal frequency.
2. Synchronize the line and frame rate of television broadcasts.
3. Even moderate the tunes of different octaves with electronic organs.
4. Used to hold output voltages in its unstable state for a certain period of time.
5. The monostable multivibrator is used as delay and timing circuits.
6. It is also used for temporary memories.
7. It is often used to trigger another pulse generator.
8. It is used for regenerating old and worn out pulses.
9. Used in amateur radio equipment to receive and transmit radio signals.
10. Used in Morse code generators, timers, and systems that require a square wave, including television broadcasts and analog circuits.
11. Involve in radio gears to transmit and receive radio signals and also in time, morse code generators and some systems which require a square wave like analog integrated circuits and TV broadcasts.
12. The astable or free running multivibrator is used as a square wave frequency generator
13. As a timing oscillator or clock of a computer system.
14. It is also used for flashing lights, switching and power supply circuits.
15. Amateur radio equipment to receive and transmit radio signals.
16. Used in Morse code generators.
17. Timers.

18. Systems that require a square wave, including television broadcasts and analog circuits.

EXPT NO: 13

BISTABLE MULTIVIBRATOR AND SCHMITT TRIGGER

AIM:

To design a fixed bias Bistable Multivibrator and to measure the stable state voltages before and after triggering.

APPARATUS REQUIRED :

1. Multisim software version 12.0
2. Operating system windows XP
3. PC

THEORY:

A Bistablemultivibrator has two stable output states. It can remain indefinitely in any one of the two stable states, and it can be induced to make an abrupt transition to the other stable state by means of suitable external excitation. It would remain indefinitely in this stable state, until it is again induced to switch into the original stable state by external triggering.

Bistablemultivibrators are also termed as 'Binary's or Flip-flops'**.** A binary is sometimes referred to as ***'Eccles-Jordan Circuit'***.

Principle of Operation of bistable multivibrator:

Consider the circuit as shown in the figure.1. The transistor Q_1 and Q_2 are n-p-n transistors. They are coupled to each other as shown in figure 1. It is evident that the output of each transistor is coupled to the input of the other transistor. Since the transistors are identical, there quiescent currents would be the same, unless the loop gain is greater than unity. When I_1 increases slightly, the voltage drop across the collector resistance R_{C1}increases. Since $V_{CC}$is fixed, the voltage of point C decreases. This has the effect of decreasing the base current of Q_2. This, in turn, decreases the collector current of Q_2viz. I_2 decreases, the voltage dropI_2R_{C2} decreases. Hence the voltage of point *D* increases.

Due to increase of V_D, the base current of Q_1 increases. This increases the collector current of Q_1vizI_1. Thus I_1 further increases. I_1R_{C1} drop further increases, V_C further decreases, the base current of Q_2 further decreases, with the result that I_2 further decreases. Thus it can easily seen that if the collector current I_1 increases even marginally, I_2 would go on progressively decreasing and as a result, I_1 would progressively increase. Eventually I_2 would become practically zero, cutting off the transistor Q_2, at the same time transistor Q_1 would conduct heavily with the result that it would be driven into saturation. Thus Q_2 becomes OFF and Q_1 becomes ON. It can similarly be shown that if I_2 increases even marginally similar sequence of operation would result and ultimately Q_2 would be ON and Q_1 OFF. Thus when Q_1 is ON, Q_2 is OFF and when Q_1 is OFF Q_2 is ON.

CIRCUIT DIAGRAM:

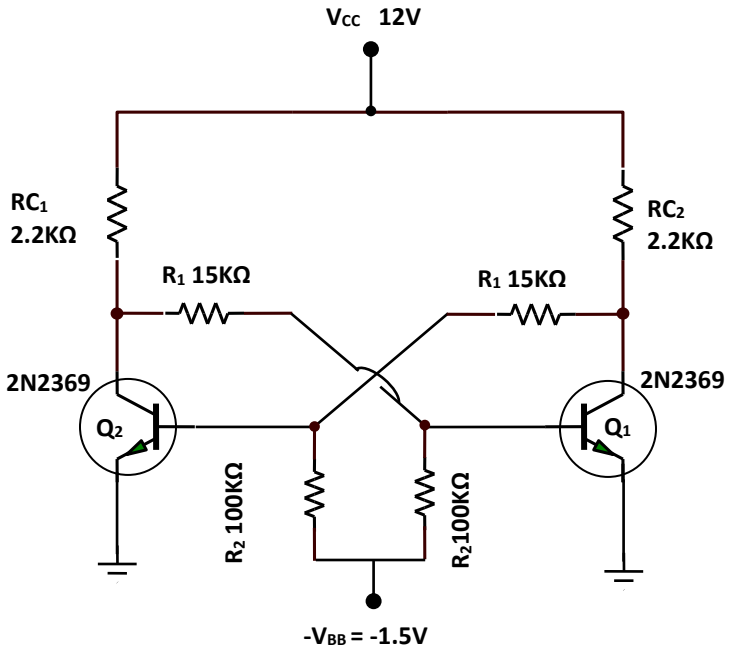


Figure: 2

PROCEDURE:

1. Connect the circuit as shown in figure 2.
2. Observe the waveforms at V_{BE1}, V_{BE2}, V_{CE1}, V_{CE2} using CRO &multimeter
3. Observe the voltages at V_{C1} and V_{C2}.
4. If $V_{C1=}$ $V_{CE(Sat)}$ and $V_{C2=}V_{CC}$(Approximately) then Q1 is 'ON' and Q2 is 'OFF' Otherwise $V_{C1=}$ V_{CC} (Approximately) and $V_{C2=}$ $V_{CE(Sat)}$) then Q1 is'OFF' and Q2 is'ON'.
5. Observe which transistor is in ON state and which transistor is in OFF state. and observe the voltages V_{C1}, V_{C2}, V_{B1}, and $V_{B2.}$
6. Apply –ve triggering at the base of the ON transistor and observe the voltages V_{C1}, V_{C2}, V_{B1}, and $V_{B2.}$

OBSERVATIONS:

Before Triggering : When Q1 is ‘ON’ and Q2 is ‘OFF’

	V_{BE1}	V_{BE2}	V_{CE1}	V_{CE2}
Stable state Voltages				

After Triggering: When Q1 is‘OFF’ and Q2 is‘ON’.

	V_{BE1}	V_{BE2}	V_{CE1}	V_{CE2}
Stable state Voltages				

CONCLUSION:

Conclusion can be made on which transistor is ‘ON’ and which transistor is ‘OFF’ before triggering and after triggering.

SCHMITT TRIGGER

AIM:

To design a Schmitt trigger and to observe the waveforms for a given UTP & LTP Values and test its performance.

COMPONENTS REQUIRED:

1. Resistors
2. Transistors 2N2369 – 2

APPARATUS:

1. Bread board
2. Power supply (0-30V)
3. Signal generator(1Hz-1MHZ)
4. CRO(1Hz-20MHz)
5. Connecting Wires.

CIRCUIT DIAGRAM:

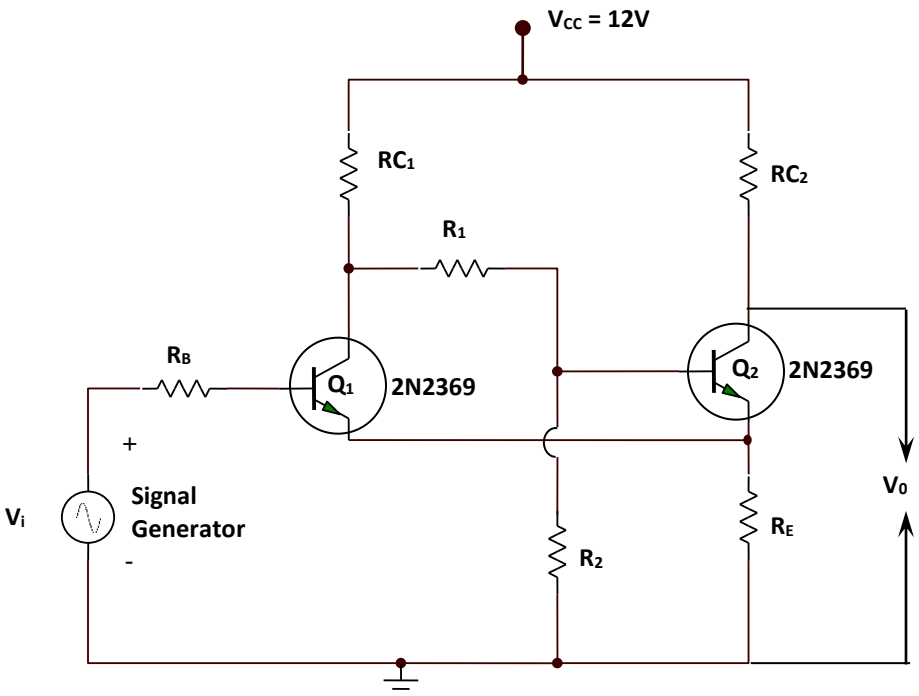


Figure:1

THEORY:

The most important application of Schmitt Trigger circuit are amplitude comparator and squaring circuit are amplitude comparator and squaring circuit. The circuit is used to obtain a square waveform from any arbitrary input waveform. The loop gain is to be less than unity.

If Q_2 is conducting there will be voltage drop across R_Z which will elevate the emitter of Q_1. Consequently if V is small enough in voltage, Q_1 will be cut-off with Q_1 conducting, the circuit amplifies and since the gain is positive, the output to rise, V_2continues to fall and Z_2 continues to rise. Therefore a value of V will be reached where Q_2 is turned OFF. At the point the output no longer responds to the input.

Here the input signal is arbitrary except that it has large enough excursion to carry input beyond the limits of hysteresis range, $V_H = (V_1 – V_2)$.

The output is a square wave whose amplitude is independent of the amplitude of the input waveform.

Design:

Given UTP=5V,LTP=3V

I_{C2} = 5mA
$(Rc_2 + R_E) = V_{CC} / I_{C2}$
U.T.P = V_{E2} = 5V
$V_{E2} = (R_E \times V_{CC}) / (Rc_2 + R_E)$
$I_2 = 0.1 \times I_{C2}$
L.T.P = V_{E1} = 3V
$R_2 = E_{R2i} / I_2 = V_{E1} / I_2$ = L.T.P / I_2

$Rc_1 = \{(R_E \times V_{CC}) / V_{E1}\} - R_E$
$I_{B2} = I_{C2} / hfe(min)$
$(V_{CC} - V_{E2}) / (R_1 + R_{c1}))) = (V_{E2}/R_2) + I_{B2}$
$R_B = (h_{fe} \times R_E) / 10$
Find R_1, R_2, R_E, $Rc_1$and Rc_2 from the above equations

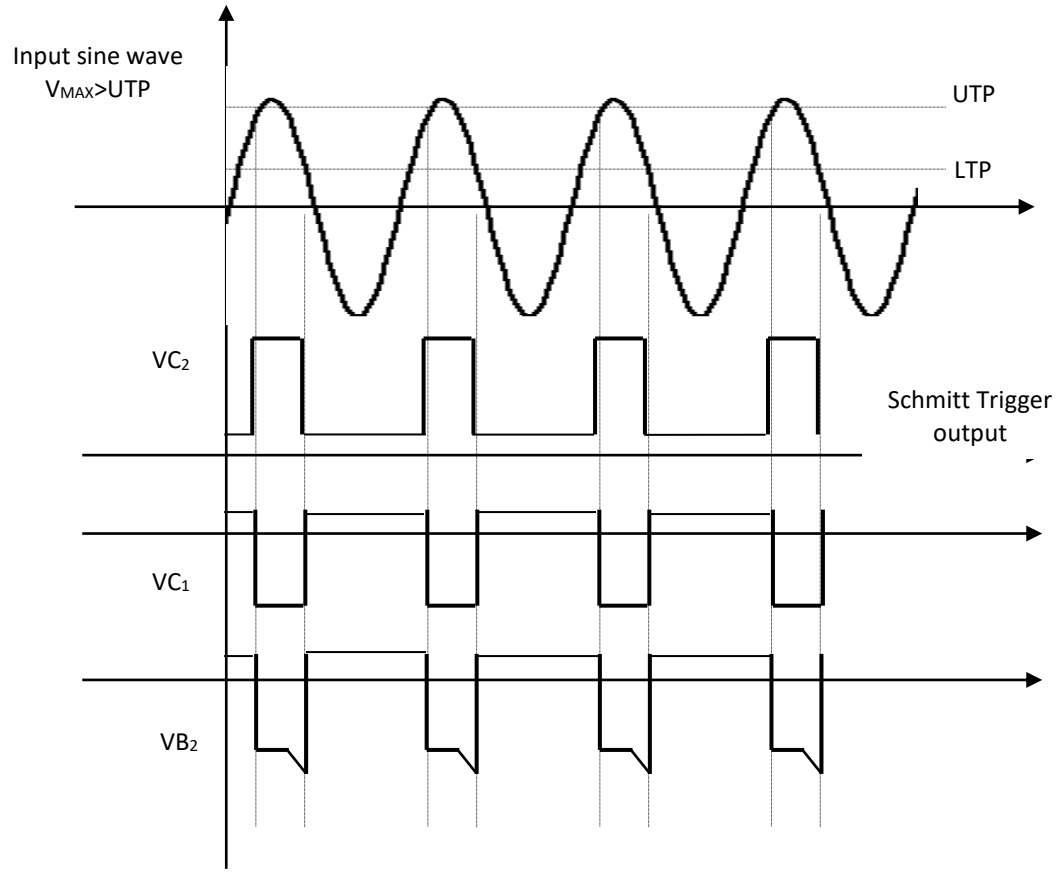
OBSERVATION TABLE:

	Theoritical Calculation			Practical Calculation
S.No	UpperthresholdPoint(U.T.P) $= + Vsat(+V_{CC}) * \frac{R2}{R1+R2}$	LowerthresholdPoint(L.T.P) $= - Vsat(-V_{CC}) * \frac{R2}{R1+R2}$	$Hysistersis(V_H)$= U.T.P - L.T.P	$Hysistersis(V_H)$= U.T.P - L.T.P
1				

PROCEDURE:

1. Connect the circuit as shown in figure 1 with designed values.
2. Apply V_{CC} of 12V and an input frequency of 1KHz with an amplitude more than the designed UTP.
3. Now note down the output wave forms
4. Observe that the output comes to ON state when input exceeds UTP and it comes to OFF state when input comes below LTP
5. Observe the waveforms at V_{C1}, V_{C2}, V_{B2} and V_E and plot graphs.
6. Keep the DC- AC control of the Oscilloscope in DC mode.

MODEL GRAPHS:



CONCLUSIONS:

Conclusion can be made on desined and practical values of U.T.P and L.T.P. and also made on output waveform of Schmitt trigger for the given sinusoidal input.

DESIGN PROBLEMS:

1. Determine UTP and LTP of a Schmitt trigger having the values , $R_1=R_2=18K$, $Rc_1=Rc_2=2.7K$, $R_E=1.5K$
2. Design a Schmitt Trigger using npn transistor for Vcc=12 V, UTP=3.5V, LTP=2.5V ,hfe=50,Ic2=2mA
3. Determine UTP and LTP of a Schmitt trigger having the values , $R_1=R_2=10K$, $Rc_1=Rc_2=3.3K$, $R_E=4.7K$
4. Design a Schmitt Trigger using npn transistor for Vcc=10 V, UTP=5.5V, LTP=2.5V ,hfe=50,Ic2=3mA
5. Design a Schmitt trigger for the Hysteresis of 3V
6. Determine UTP and LTP of a Schmitt trigger having the values , $R_1=R_2=18K$, $Rc_1=Rc_2=2.7K$, $R_E=1.5K$

7. Design a Schmitt Trigger using npn transistor for Vcc=12 V, UTP=5V, LTP=4.5V ,hfe=50,Ic2=1.5mA
8. Determine UTP and LTP of a Schmitt trigger having the values , $R_1=R_2=15K$, $Rc_1=Rc_2=3K$, $R_E=4K$
9. Design a Schmitt Trigger using npn transistor for Vcc=10 V, UTP=5.5V, LTP=2.5V ,hfe=50,Ic2=3mA
10. Design a Schmitt trigger for the Hysteresis of 7V
11. Design a Bistable multivibrator with Vcc=10V, $R_1=2K$, $R_2=20K$, $Rc_1=Rc_2=2K$, C=0.1µF at Vin=8V
12. Design a Fixed Bias Binary multivibrator with Vcc=12V, $R_1=2K$, $R_2=20K$, $Rc_1=Rc_2=2K$, C=0.1µF at Vin=4V
13. Design a Bistable multivibrator with Vcc=10V, $R_1=5K$, $R_2=20K$, $Rc_1=Rc_2=2K$, C=0.1µF at Vin=8V
14. Design a Bistable multivibrator with Vcc=10V, $R_1=2K$, $R_2=15K$, $Rc_1=Rc_2=4K$, C=0.1µF at Vin=10V
15. Design a Fixed Bias Binary multivibrator with Vcc=10V, $R_1=3K$, $R_2=25K$, $Rc_1=Rc_2=2K$, C=10µF at Vin=5V
16. Design a flip flop or Binary with BFW10 and $R_1=2K$, $R_2=20K$, $Rc_1=Rc_2=2K$, C=0.1µF at Vin=8V
17. Design a flip flop or Binary with BFW10 and $R_1=5K$, $R_2=20K$, $Rc_1=Rc_2=2K$, C=0.1µF at Vin=8V
18. Design a Bistablemultivibrator with Vcc=10V, $R_1=2K$, $R_2=15K$, $Rc_1=Rc_2=4K$, C=0.1µF at Vin=10V
19. Design a Bistablemultivibrator with Vcc=10V, $R_1=2K$, $R_2=20K$, $Rc_1=Rc_2=2K$, C=0.1µF at Vin=8V with commutating capacitors $C_1=C_2=1µF$
20. Design a Bistable multivibrator with Vcc=10V, $R_1=2K$, $R_2=20K$, $Rc_1=Rc_2=2K$, C=10µF at Vin=8V with commutating capacitors $C_1=C_2=0.1µF$

VIVA QUESTIONS:

1. Explain how a Schmitt trigger acts as a comparator?
2. Derive its expressions for UTP & LTP.
3. What are the applications of Schmitt Trigger?
4. Define hysteresis action?
5. Why is Schmitt Trigger called a squaring circuit?
6. What is UTP?
7. What is LTP?
8. What is the difference between a Binary and Schmitt Trigger?
9. Other names of Schmitt trigger.
10. Difference between comparator and Schmitt trigger.
11. Difference between Schmitt trigger and Multivibrator.
12. For good Schmitt trigger the hysteresis value always?
13. What is Multivibrator? Explain the principle on which it works? Why is it called a binary?
14. Explain the role of commutating capacitors in a Bistable Multivibrator?
15. Give the Application of a Binary.
16. What are the applications of a Bitable multivibrator?
17. Describe the operation of commutating capacitors?
18. Why is a Binary also called a flip-flop?
19. Mention the name of different kinds of triggering used in the circuit shown?
20. What are the disadvantages of direct coupled Binary?
21. How many types of unsymmetrical triggering are there?
22. What are catching diodes?
23. Which triggering is used in binary counting circuits?
24. What are the applications of a Bitable Multivibrator?
25. Describe the operation of commutating capacitors?
26. Commutating capacitors are also called as __ or ?
27. What is the meaning of a stable state in a multi-vibrator?
28. Mention the names of different kinds of triggering used in the circuit shown?
29. What are the disadvantages of direct coupled Binary?
30. Mention the names of different kinds of triggering used in the circuit shown?

REAL TIME APPLICATIONS OF SCHMITT TRIGGER AND:

1. Squaring Circuit.
2. Sine-To-Square Comparator.
3. Amplitude comparator.
4. As Flip Flops.
5. A Comparator Circuit Which Converts Any Arbitrary Signal(Slope!=1) To Square.
6. The bistable multivibrator or Flip Flop is of great importance in digital operation in computers, digital communications.
7. It is also used for reversing to the supply to a given circuit or change supply to two circuit at regular intervals.

REAL TIME APPLICATIONS OF BISTABLE MULTIVIBRATORS :